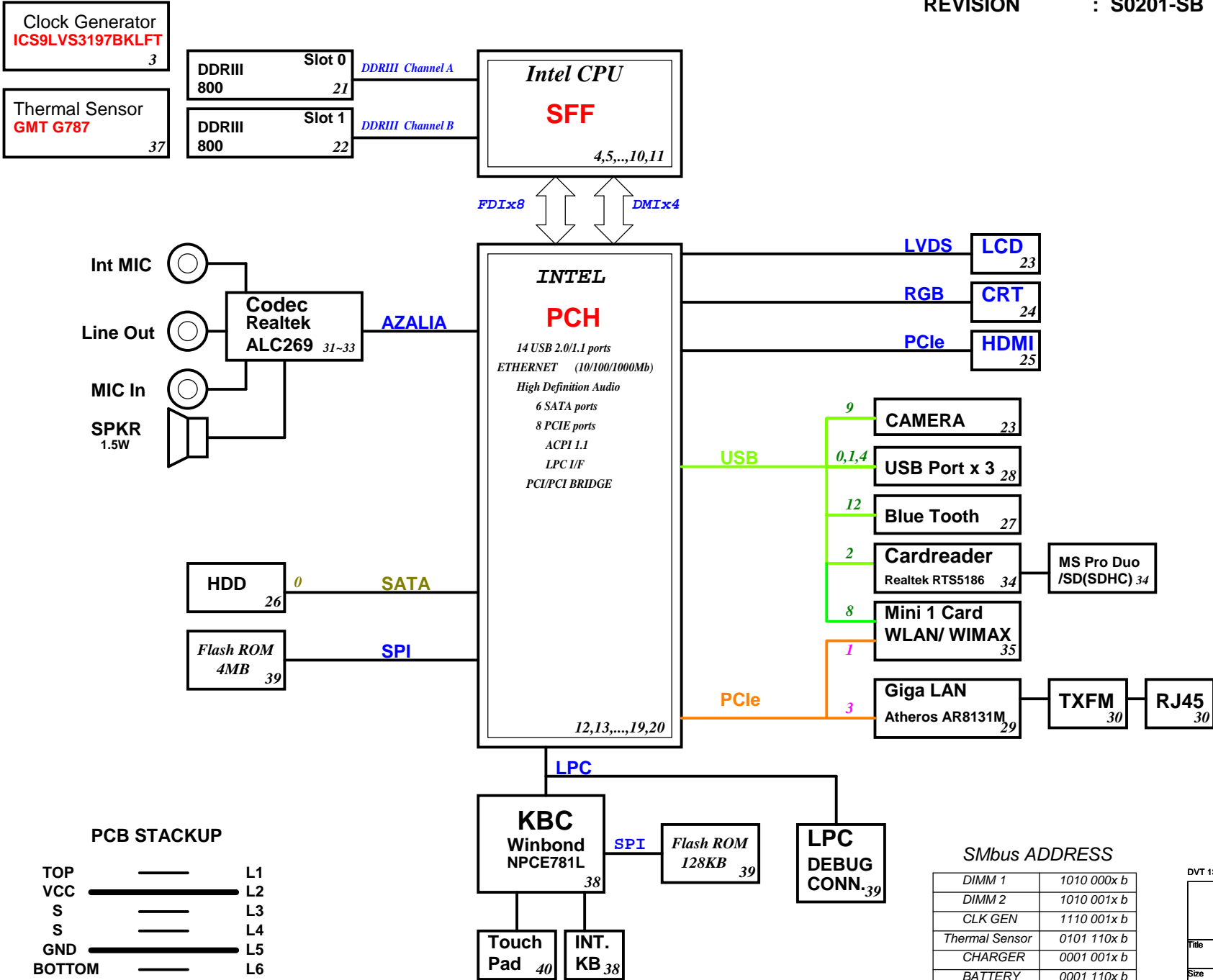


TUCANA Block Diagram

PROJECT CODE : 91.4KK01.001
PCB P/N : 48.4KK01.0SB
REVISION : S0201-SB



SYSTEM DC/DC RT8223 47	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(5A) 5V_AUX_S5 3D3V_AUX_S5
RT8209 49	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(20A)
RT8209 48	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3(9.4A)
RT9026 51	
INPUTS	OUTPUTS
5V_S5	DDR_VREF_S3 1.2A
CHARGER BQ24751 52	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A
CPU DC/DC ADP3211 46	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 27A
GFX Core ADP3211 50	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE 11A

SMbus ADDRESS

DIMM 1	1010 000x b
DIMM 2	1010 001x b
CLK GEN	1110 001x b
Thermal Sensor	0101 110x b
CHARGER	0001 001x b
BATTERY	0001 110x b

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Wistron Corporation

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Title		BLOCK DIAGRAM	
Size A3	Document Number	Rev SB	
Date: Wednesday, July 07, 2010		Sheet 1	of 56

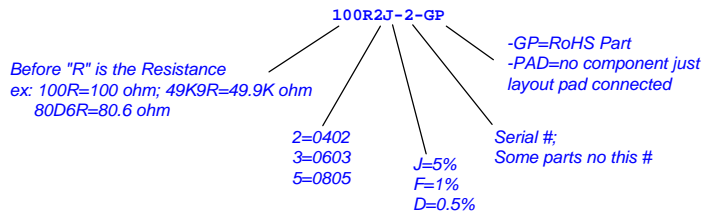
PCH Strapping

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	Default - Internal pull-up. Low (0)= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1) : Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

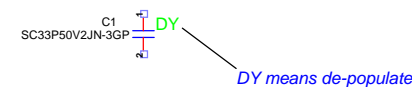
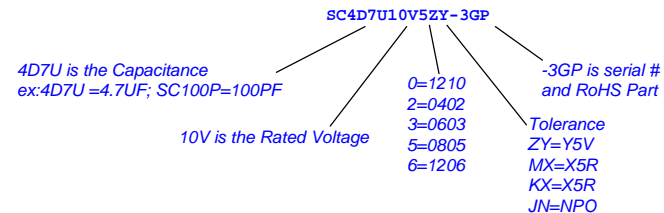
Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarksfield samples.	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (xPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

Resistor

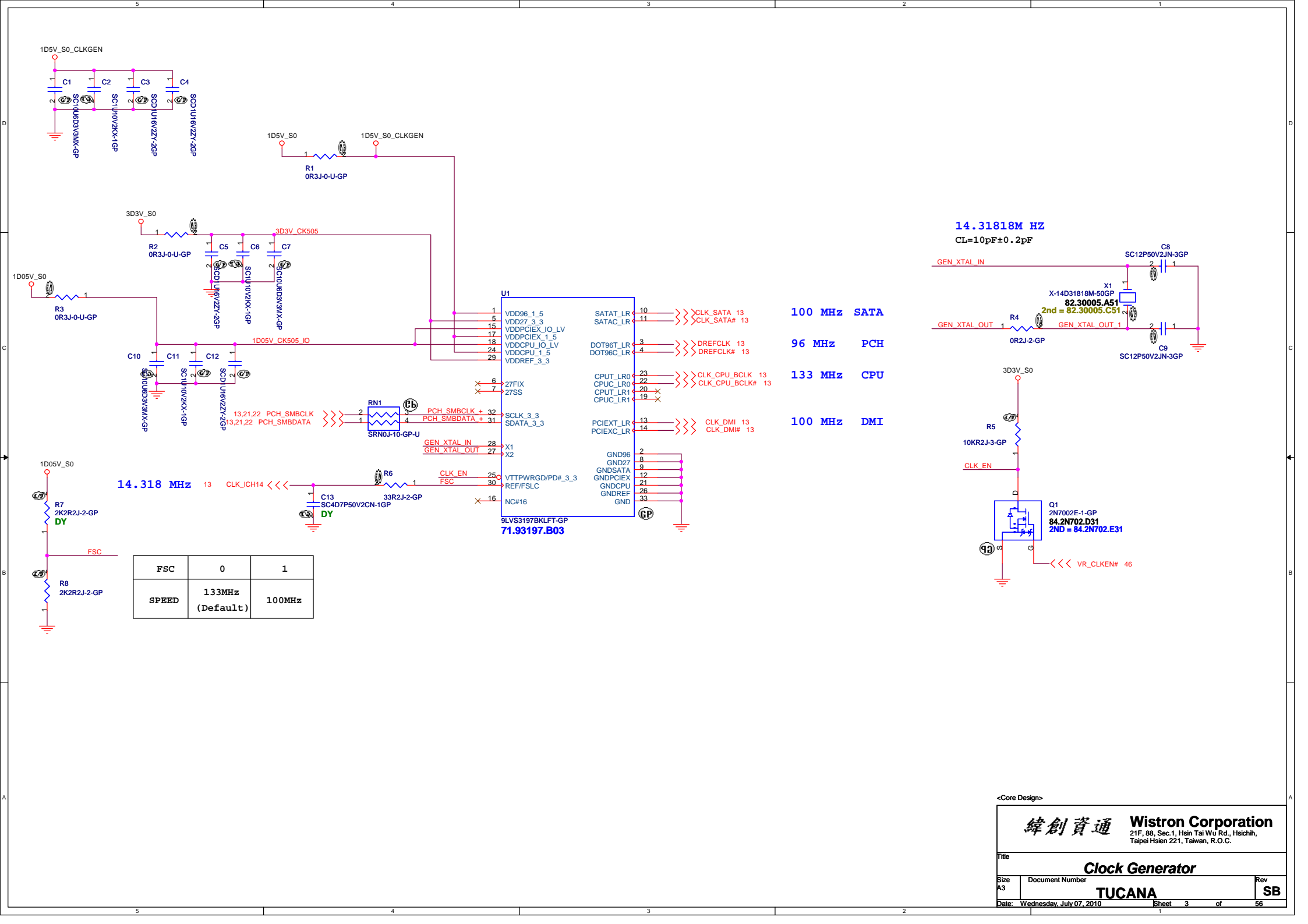


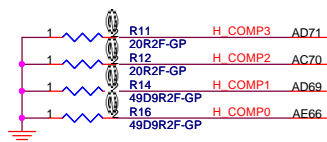
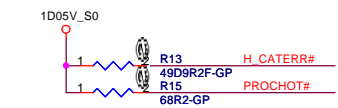
Capacitor



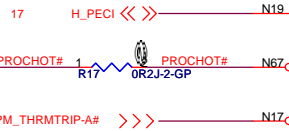
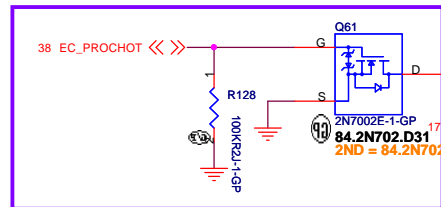
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Title			
Reference			
Size A3	Document Number	TUCANA	Rev SB
Date: Wednesday, July 07, 2010			
Sheet 2 of 56			





DVT 2010702



From PCH

14 PM_DRAM_PWRGD >>>

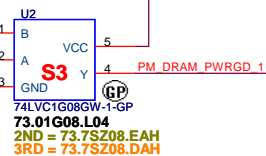
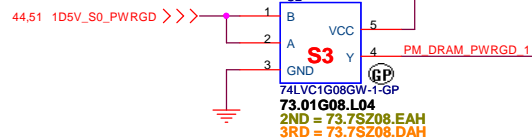
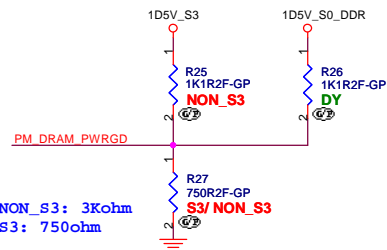
49 H_VTTPWRGD >>>

16,29,34,35,38,39,44 PLT_RST# >>>

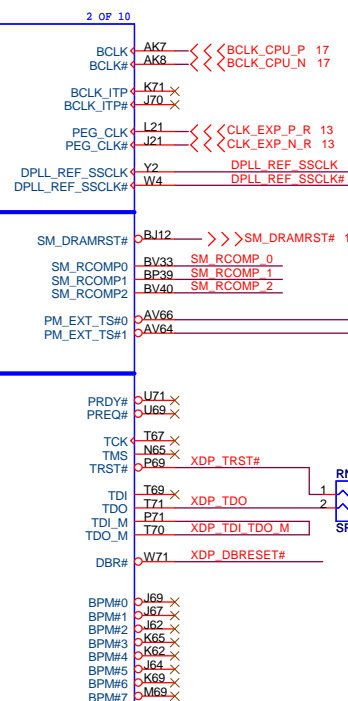
1K5R2F-2-GP

R23 750R2F-GP

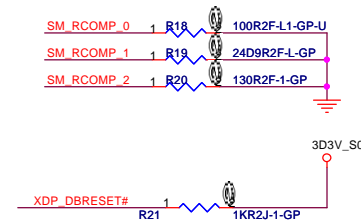
PM_DRAM_PWRGD 1 1K5R2F-2-GP PM_DRAM_PWRGD 1
S3

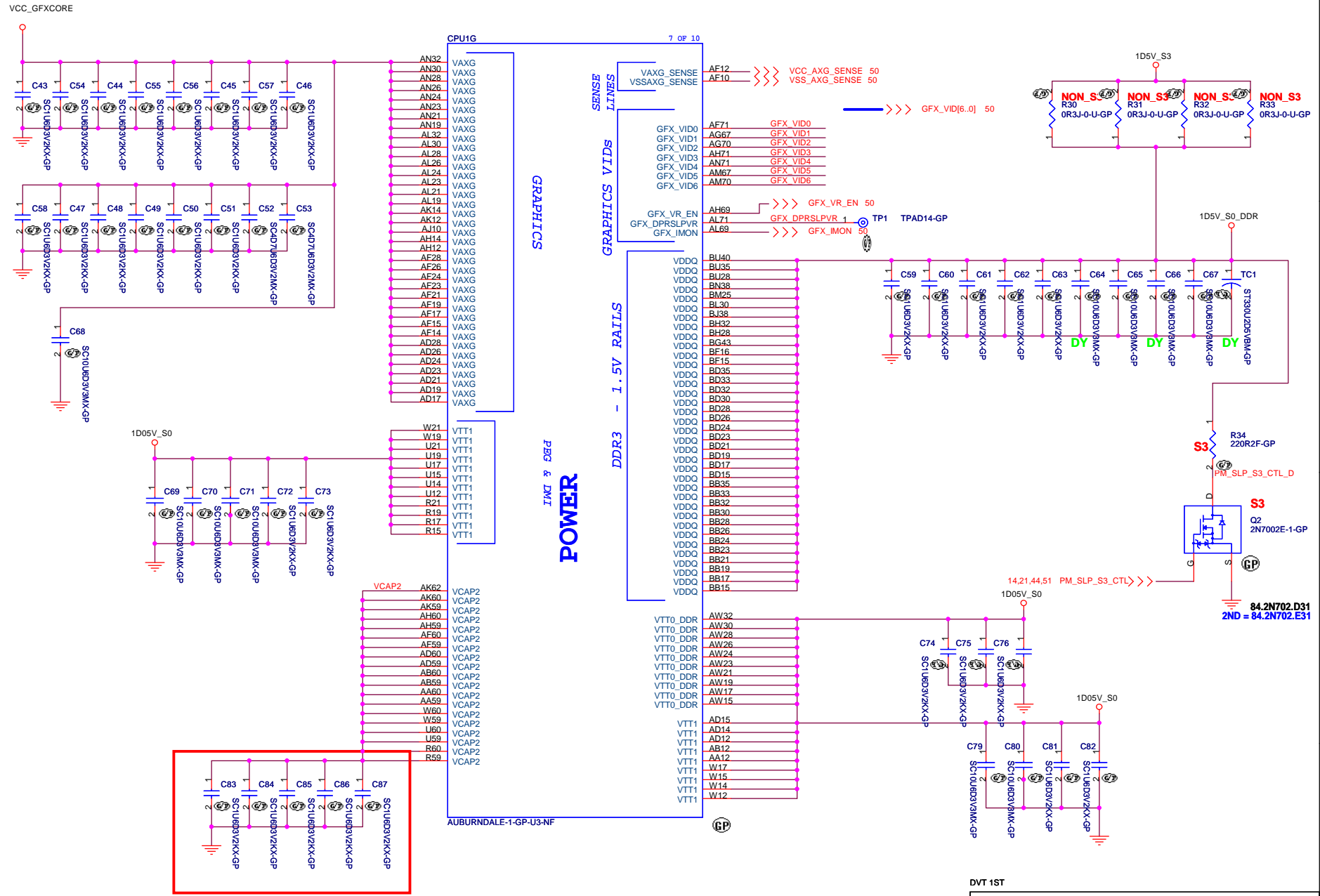


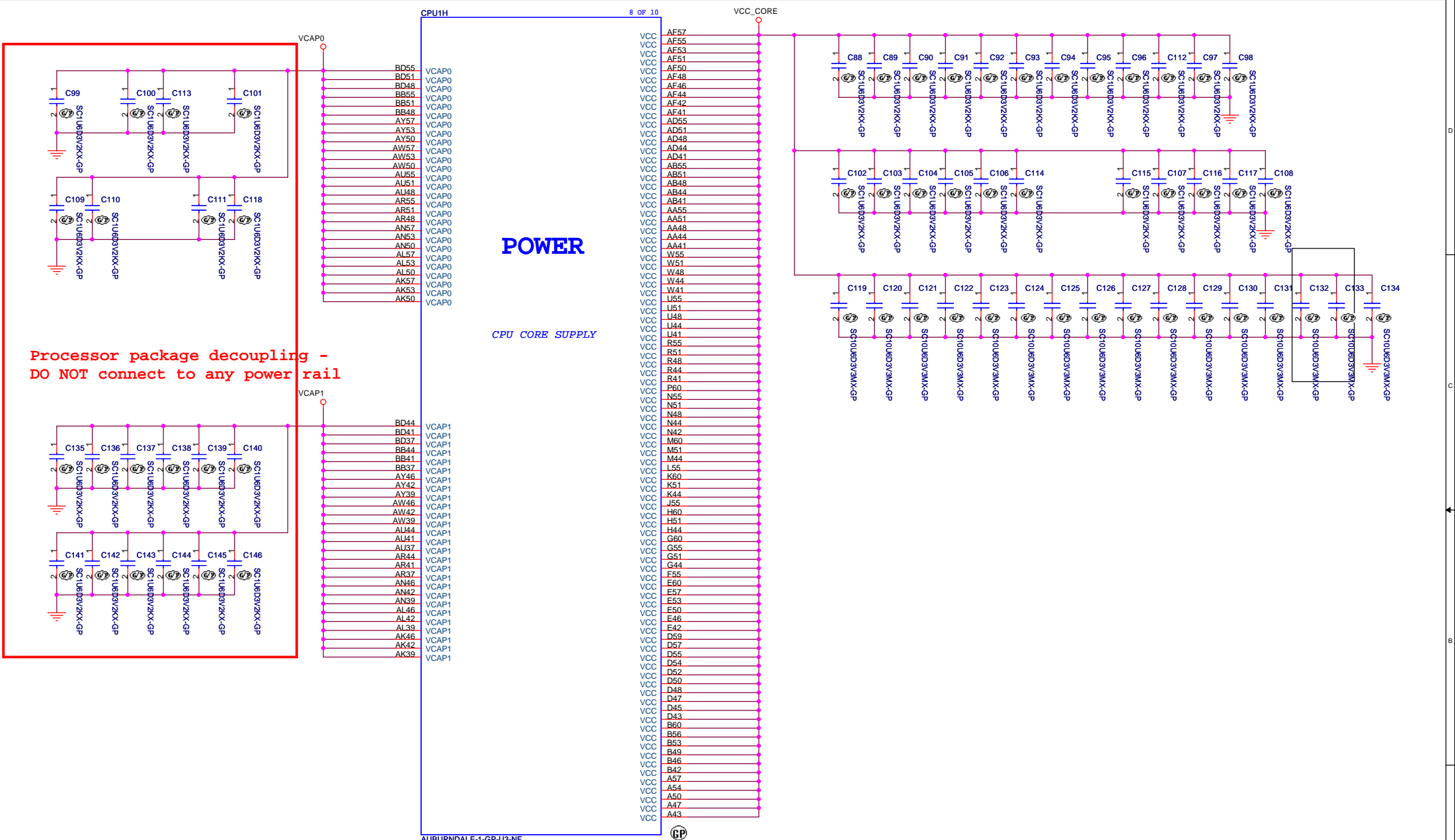
Misc
Clocks
Thermal
DDR3
Misc
Power Management
JTAG & MBP



If supports integrated graphics but without Embedded DisplayPort(eDP), these pins can also be connected to GND directly.







Processor package decoupling -
DO NOT connect to any power rail

POWER
CPU CORE SUPPLY

CPU1E

5 OF 10

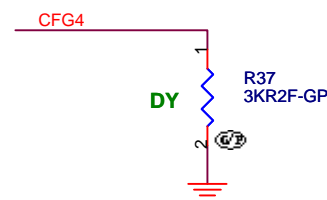
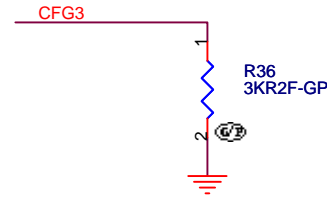
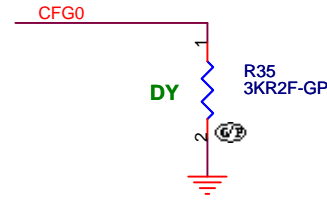
RSVD#W66
RSVD#W64W66
W64RSVD#AC69
RSVD#AC71AC69
AC71RSVD#AA71
RSVD#AA69AA71
AA69RSVD#R66
RSVD#R64R66
R64RSVD_NCTF#BT5
RSDV_NCTF#BR5BT5
BR5RSDV_NCTF#BV6
RSDV_NCTF#BV8BV6
BV8RSVD#AV69
RSVD#AK71AV69
AK71RSVD#AN69
RSVD#AP66AN69
AP66RSVD#AH66
RSVD#AK66AH66
AK66RSVD#AR71
RSVD#AM66AR71
AM66RSVD#AK69
RSVD#AU71AK69
AU71RSVD#AT70
RSVD#AR69AT70
AR69RSVD#AU69
RSVD#AT67AU69
AT67RSVD_TP2
RSVD_TP1AP2
AN7RSVD#AV4
RSVD#AU2AV4
AU2RSVD#BE69
RSVD#BE71BE69
BE71

RESERVED

NCTF TEST PIN:

A5,A68,A69,A71,C3,C71,E1,E71,BR1,BR71,
BT1,BT71,BV1,BV3,BV5,BV68,BV69,BV71NCTF_DC_TEST#BV71
NCTF_DC_TEST#BV69
NCTF_DC_TEST#BV68
NCTF_DC_TEST#BV5
NCTF_DC_TEST#BV3
NCTF_DC_TEST#BV1
NCTF_DC_TEST#BT71
DC_TEST_BT69
DC_TEST_BT3
NCTF_DC_TEST#BT1
NCTF_DC_TEST#BR71
NCTF_DC_TEST#BR1
NCTF_DC_TEST#E71
NCTF_DC_TEST#E1
NCTF_DC_TEST#C71
DC_TEST_C69
NCTF_DC_TEST#C3
NCTF_DC_TEST#A71
NCTF_DC_TEST#A69
NCTF_DC_TEST#A68
NCTF_DC_TEST#A5BV71 1 TP2
TPAD14-GP
BV69
BV68
BV5
BV3
BV1 1 TP3
TPAD14-GP
BT71
BT69
BT3
BT1
BR71
BR1
E71 1 TP4
TPAD14-GP
C71
C69
C3
A71 1 TP5
TPAD14-GP
A69
A68
A5

GP



PCI-Express Configuration Select

CFG0
1:Single PEG
0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal

CFG3
1 :Normal Operation
0 :Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

CFG4
1:Disabled; No Physical Display Port
attached to Embedded Display Port
0:Enabled; An external Display Port
device is connected to the Embedded
Display Port

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Title CPU SFF 7 of 8(REERVED)

Size A4 Document Number

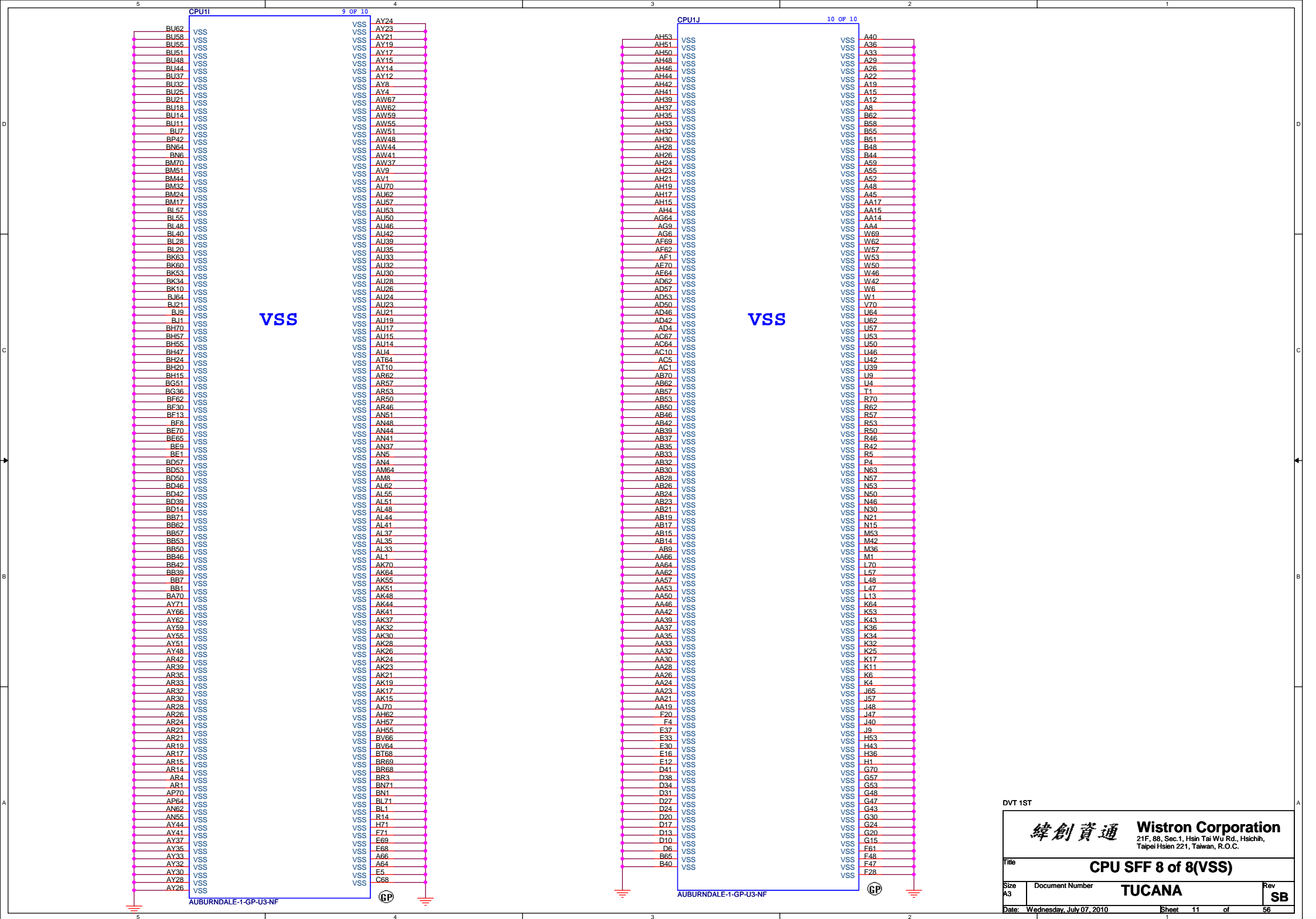
TUCANA

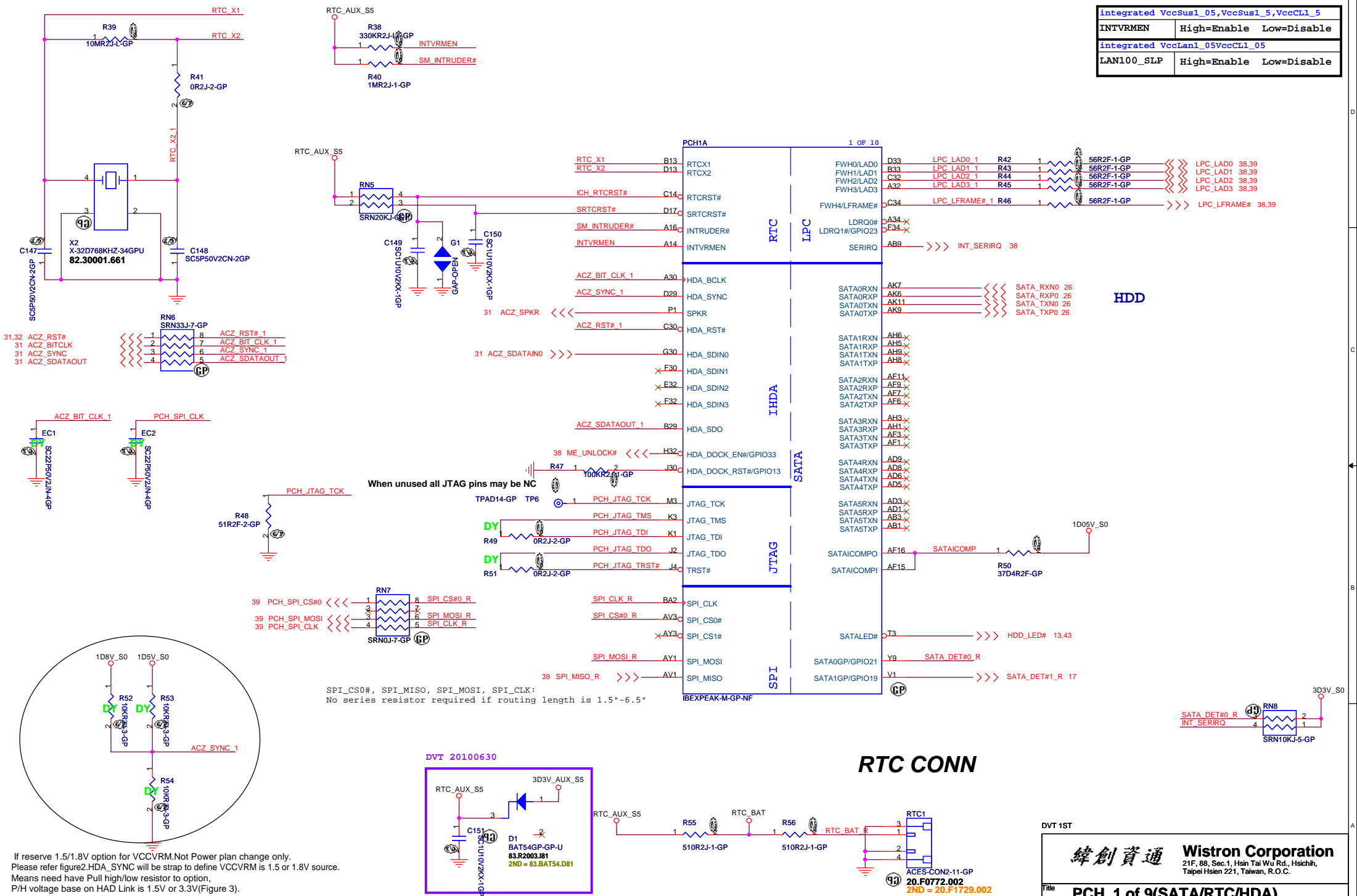
Rev

SB

Date: Wednesday, July 07, 2010

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If reserve 1.5/1.8V option for VCCVRM. Not Power plan change only.
Please refer figure2.HDA_SYNC will be strap to define VCCVRM is 1.5 or 1.8V source.
Means need have Pull high/low resistor to option,
P/H voltage base on HAD Link is 1.5V or 3.3V(Figure 3).

RTC CONN

MINICARD1-WLAN

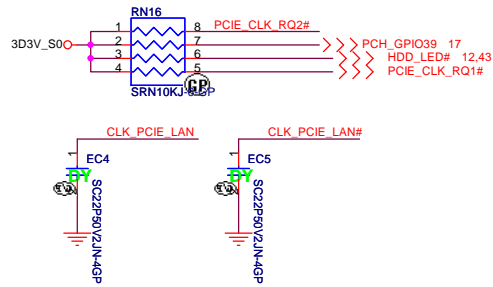
LAN

MINICARD1-WLAN

LAN

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.

PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).



PCH1B

2 OF 10

PCI-E*

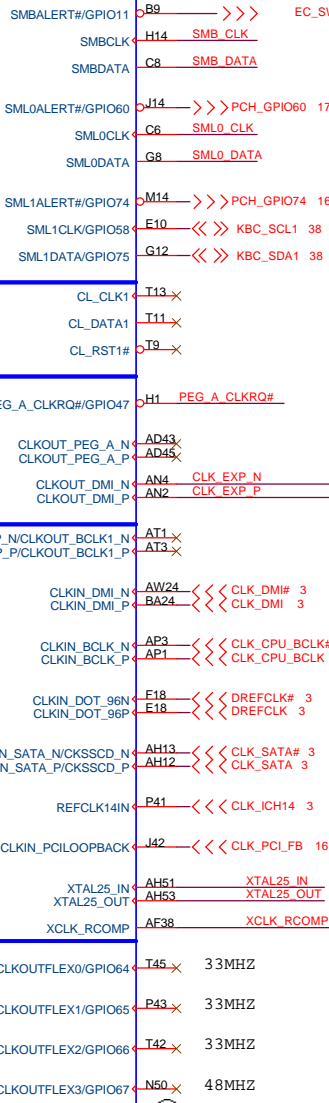
Controller

Link

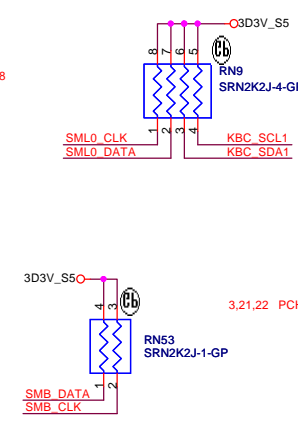
From CLK BUFFER

Clock Flex

IBEXPEAK-M-GP-NF



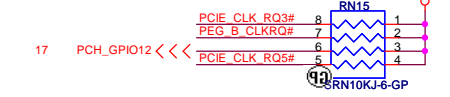
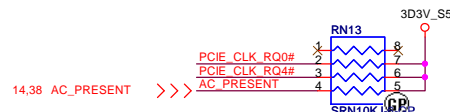
EC_SW# 14,38



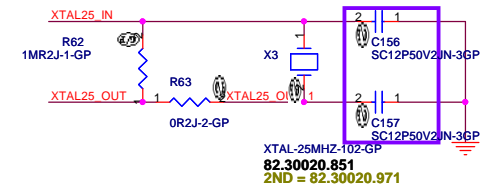
3.21,22 PCH_SMBDATA <<< >>> PCH_SMBCLK 3.21,22

CLK_EXP_N_R 5
CLK_EXP_P_R 5

1D05V_S0



DVT 20100625
Change C156,C157 to 12pF
for Crystal vendor Test

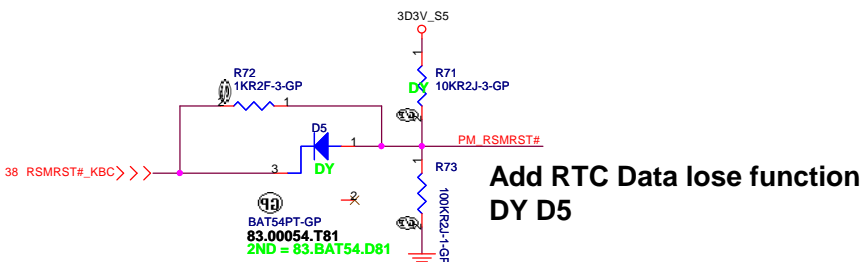
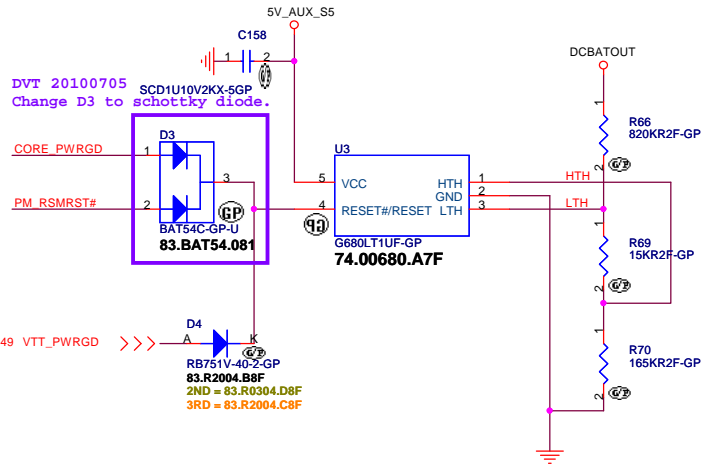


<Core Design>

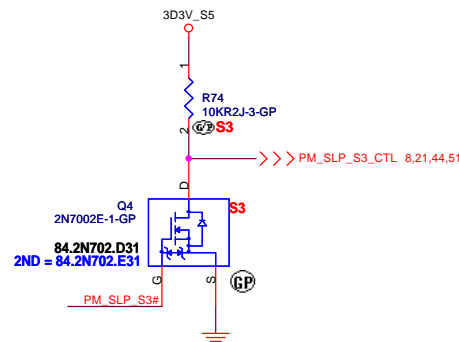
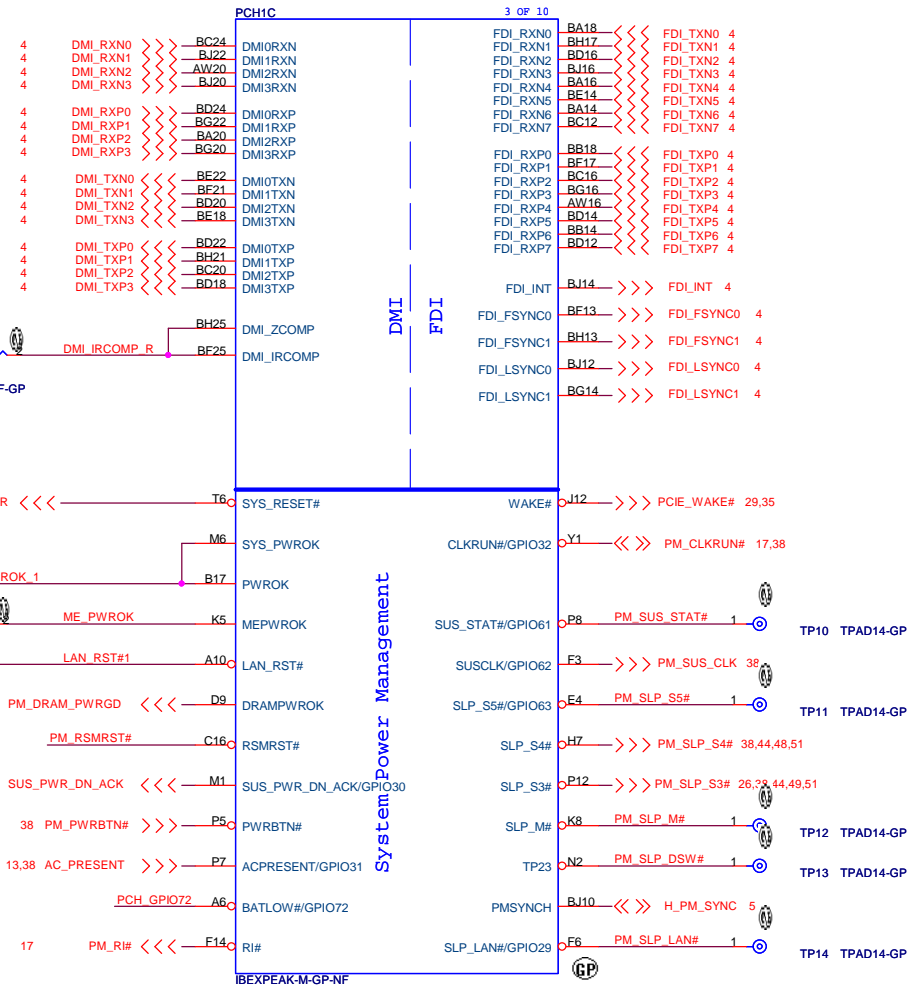
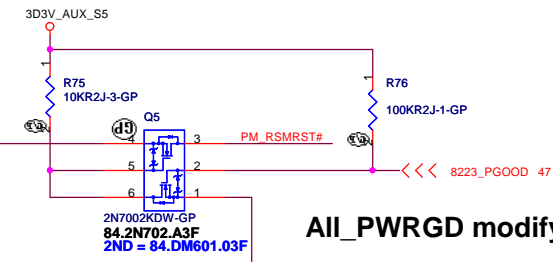
緯創資通 Wistron Corporation	
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Title	PCH 2 of 9(PCIE/CLK/SMB)
Size A3	Document Number TUCANA
Date: Wednesday, July 07, 2010	Sheet 13 of 56
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Delete PM_PWRBTN# pull high



All_PWRGD modify 51123_PGOOD from 3V/5V power

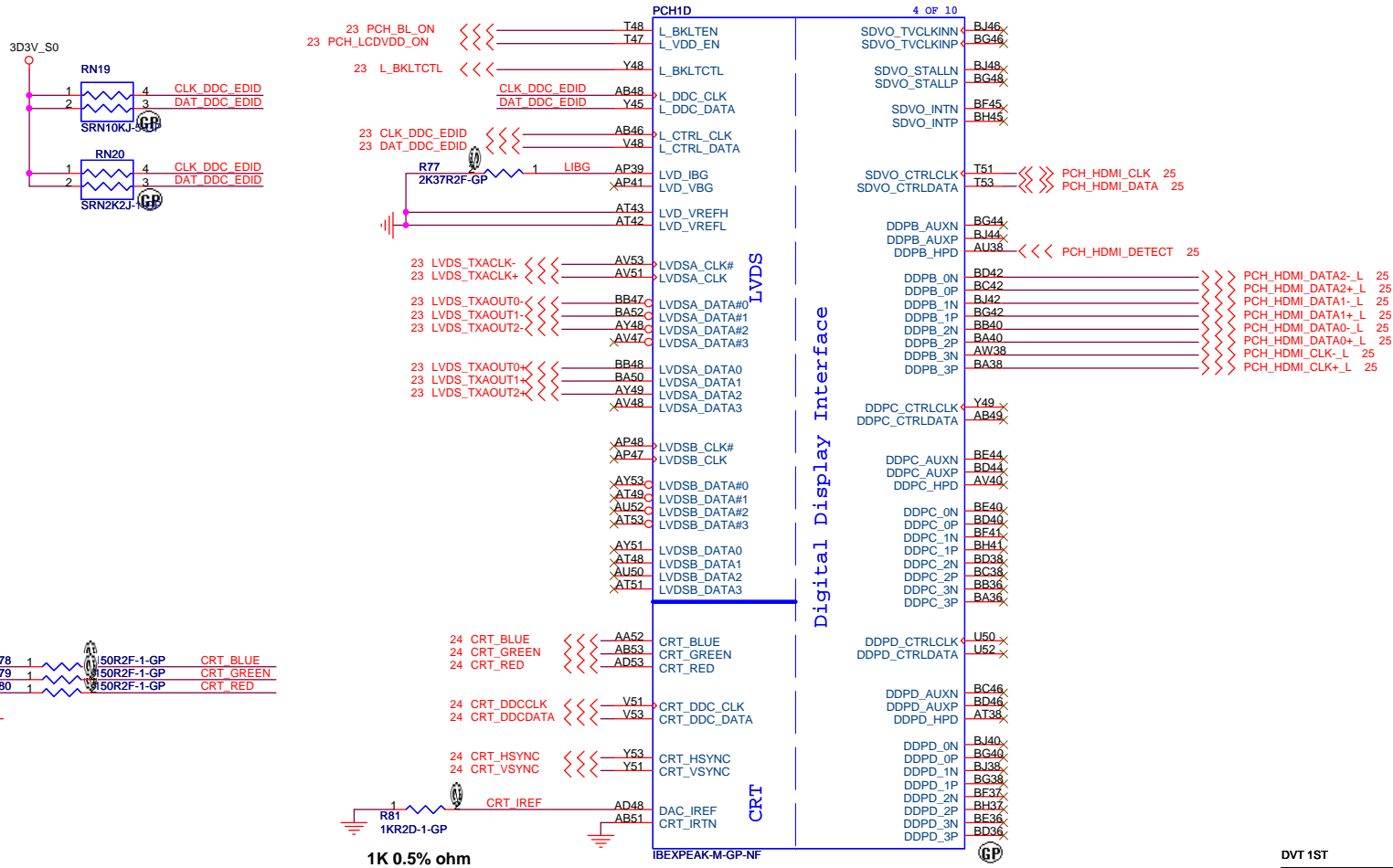


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Title		
PCH 3 of 9(DMI/FDI)		
Size	Document Number	Rev
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Date: Wednesday, July 07, 2010		Sheet 14 of 56

Panel backlight enable control for LVDS -
used to gate power into the backlight circuit



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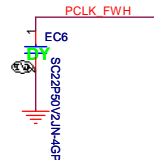
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Size Custom Document Number TUCANA Rev SB

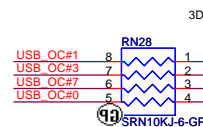
Date: Wednesday, July 07, 2010 Sheet 15 of 56



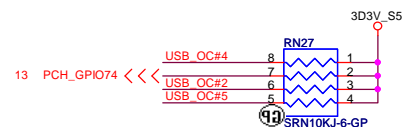
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--	---	---	-----	--



INT PIROQA#	G38	PIROA#
INT PIROB#	H61	PIROB#
INT PIROC#	B37	PIROC#
INT PIROQD#	A44	PIROQD#
PCI REQ0#	F51	REQ0#
PCI REQ1#	A46	REQ1#/GPI05#
PCI REQ2#	B53	REQ2#/GPI05#
PCI REQ3#	M65	REQ3#/GPI05A#
PCI GNT0#	F48	GNT0#
PCI GNT1#	K45	GNT1#/GPI051#
	X F36	GNT2#/GPI053#
	X H53	GNT3#/GPI055#
INT PIROFE#	B41	PIROFE#/GPI02#
INT PIROF#	A53	PIROF#/GPI03#
INT PIROGH#	A53	PIROGH#/GPI04#
INT PIROHQ#	A48	PIROHQ#/GPI05#
	X K6	PCIRST#
PCI SERR#	F44	SERR#
PCI PERR#	E50	PERR#
PCI IRDY#	A42	IRDY#
PCI DEVSLE#	X H44	PAR
PCI FRAME#	F48	DEVSLE#
	C46	FRAME#
PCI PLOCK#	D49	PLOCK#
PCI STOP#	D40	STOP#
PCI TRDY#	C41	TRDY#
	X M7	PME#
	D5	PLTRST#
CLK P1 SIO R	N52	CLKOUT_P10
CLK P1 SIO B	P53	CLKOUT_P10
CLK P1 FB R	P46	CLKOUT_P02
	X P51	CLKOUT_P03
CLK P1 KBC R	P43	CLKOUT_P04

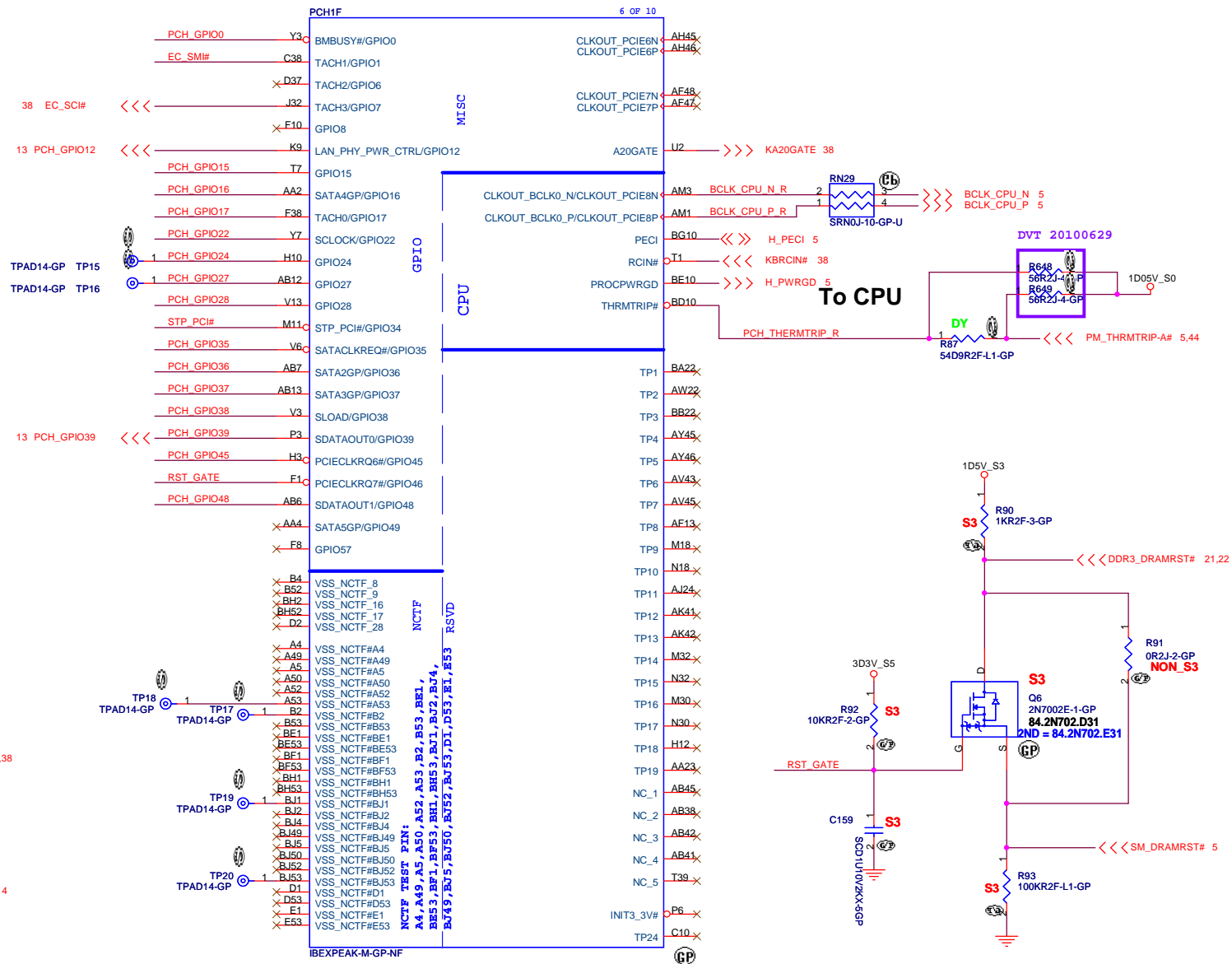
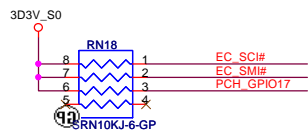


Pair	Device
0	External #0
1	External #1
2	CardReader
3	NC
4	External #2
5	NC
6	NC
7	NC
8	WLAN/WiMAX
9	CAMERA(HS)
10	NC
11	NC
12	BLUETOOTH(FS)
13	NC

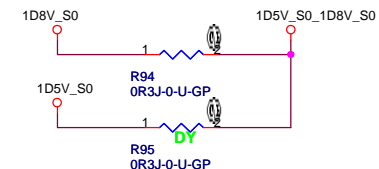
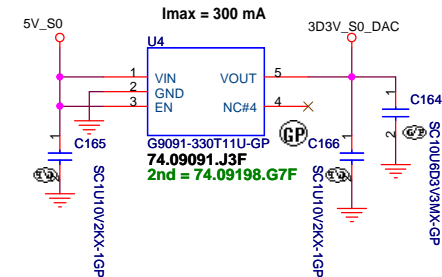
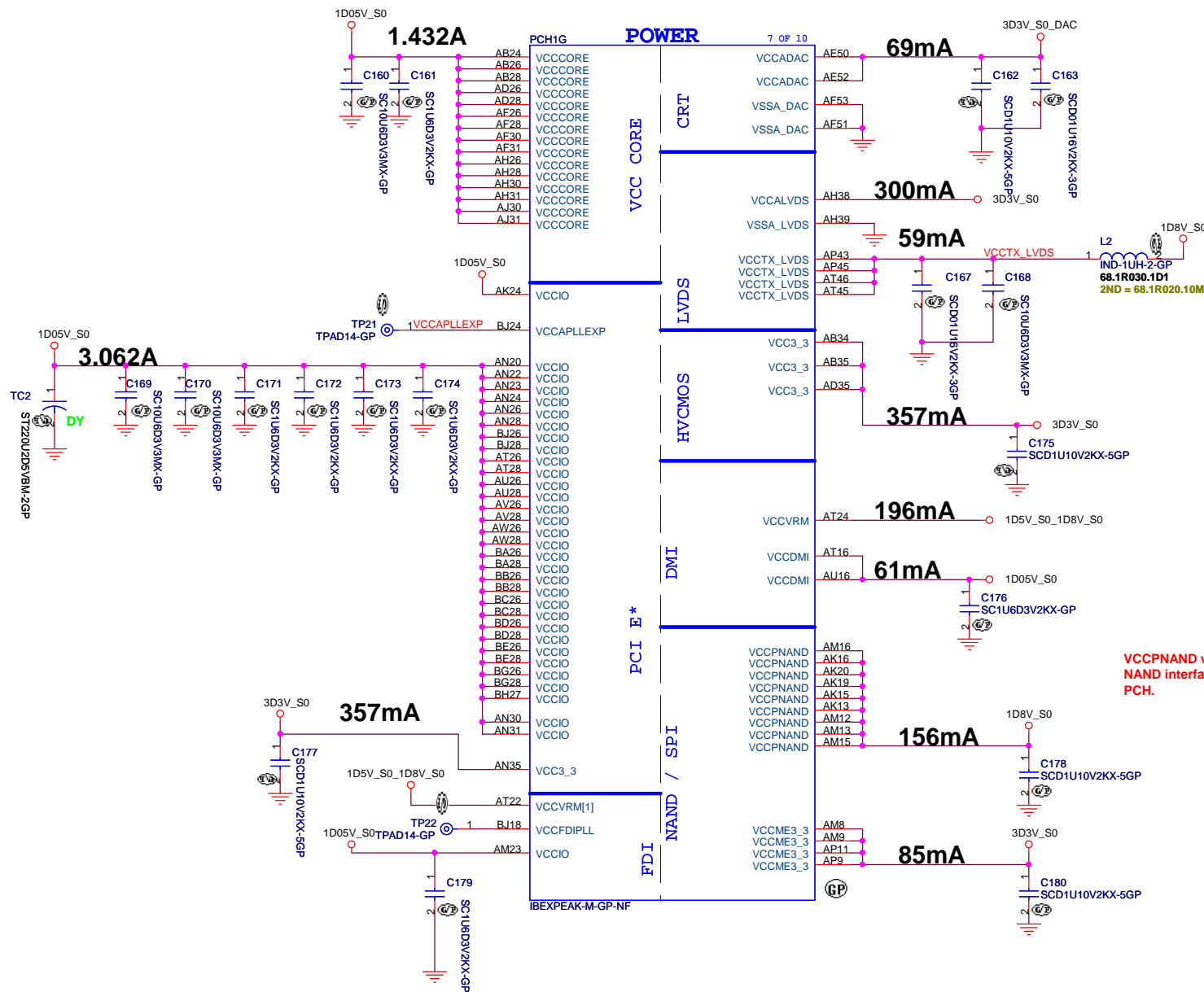


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GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regulator,
should not place external pull down.



Title				PCH 6 of 9(GPIO/RSVD)			
Size A3	Document Number					TUCANA	Rev
							SB
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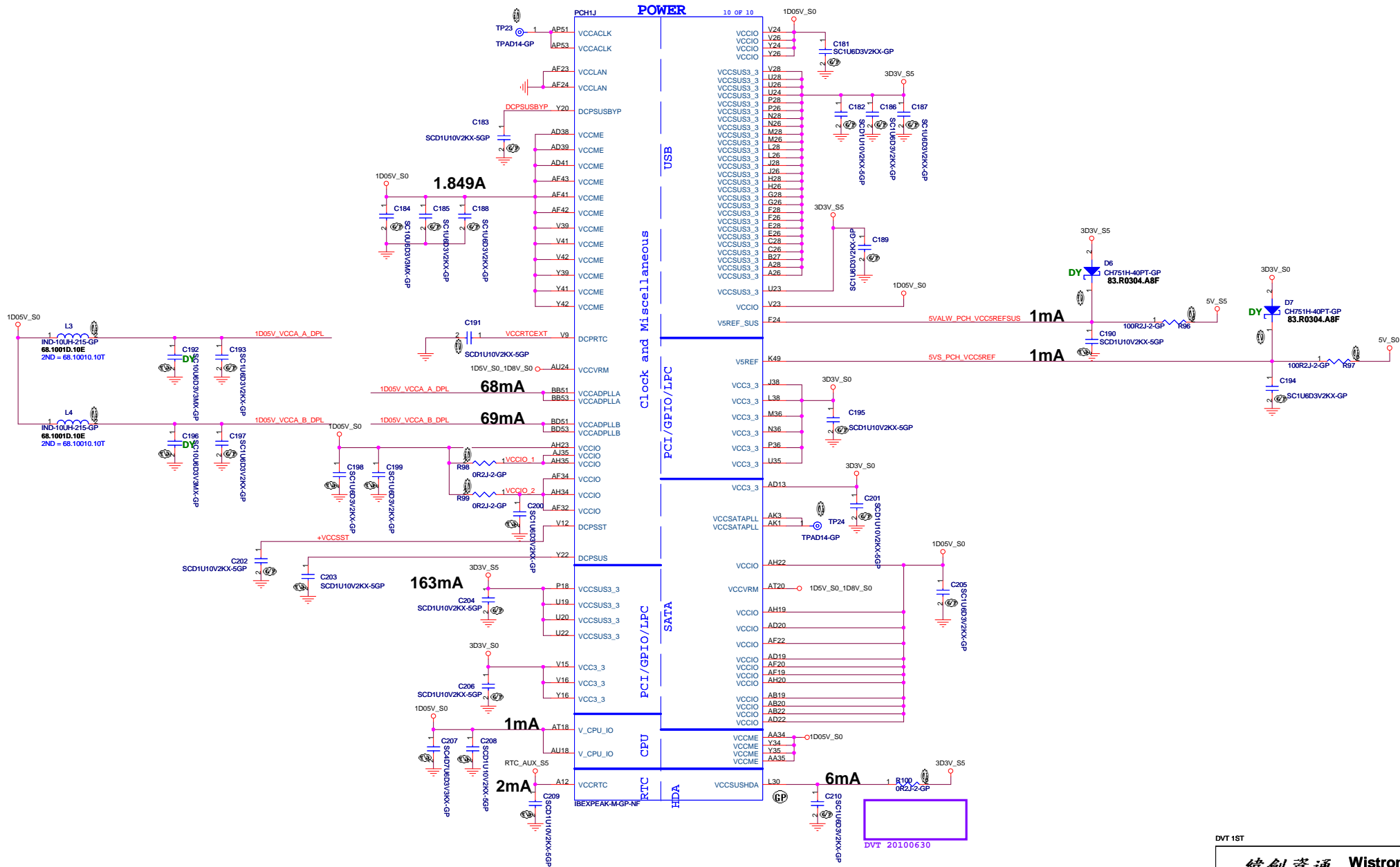


VCCPNAND which power the DC NAND interface must be powered even if dual channel NAND interface is not connected since it also supplies power to other functions inside PCH.

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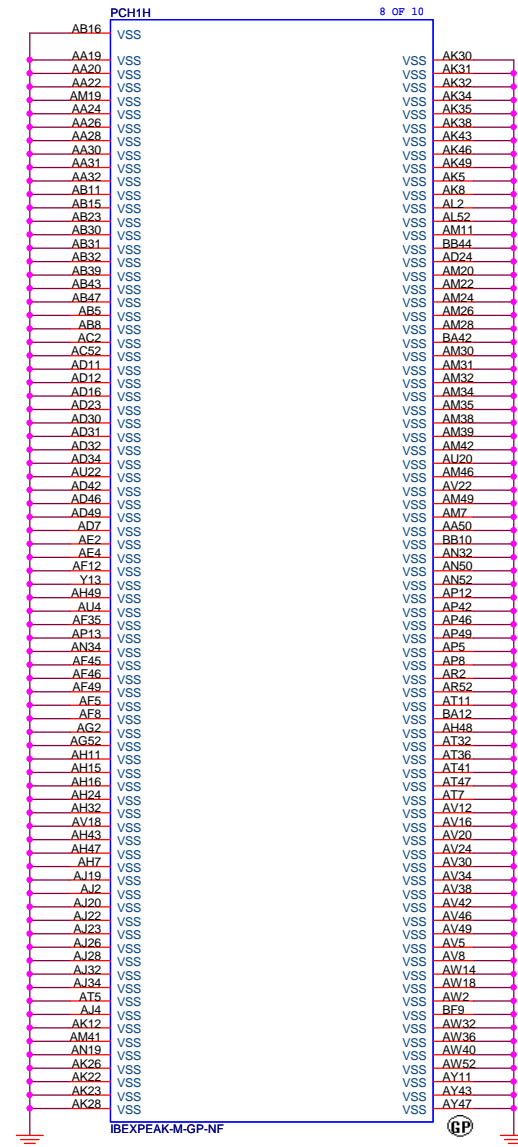
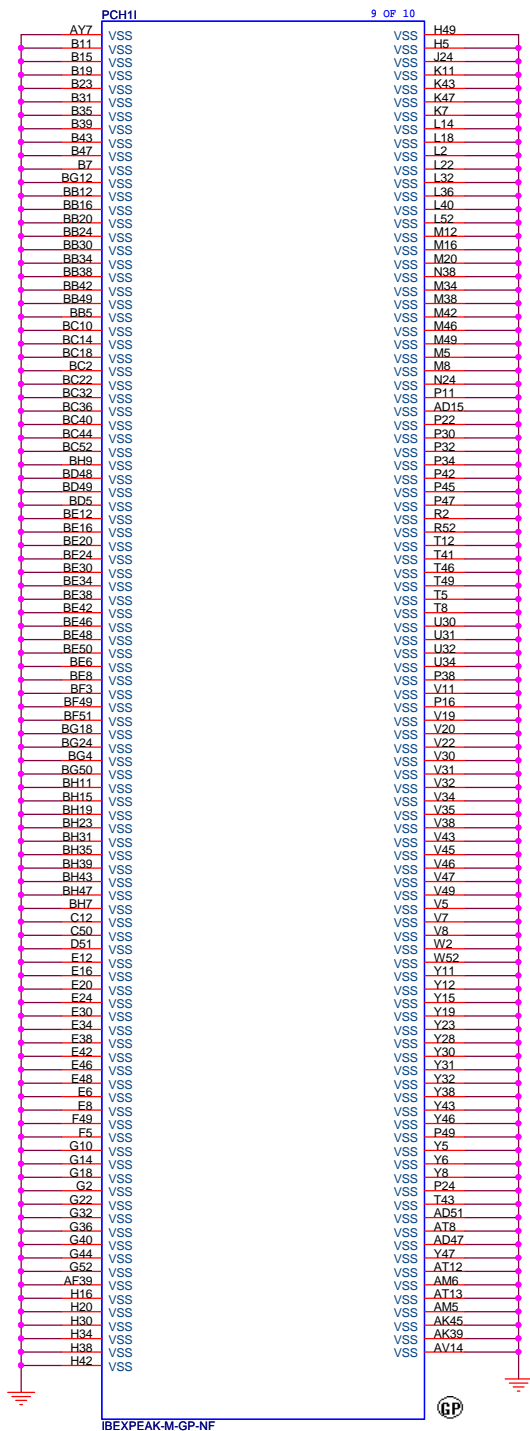
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Size Custom	Document Number TUCANA	Rev SB
Date: Wednesday, July 07, 2010	Sheet 18	of 56



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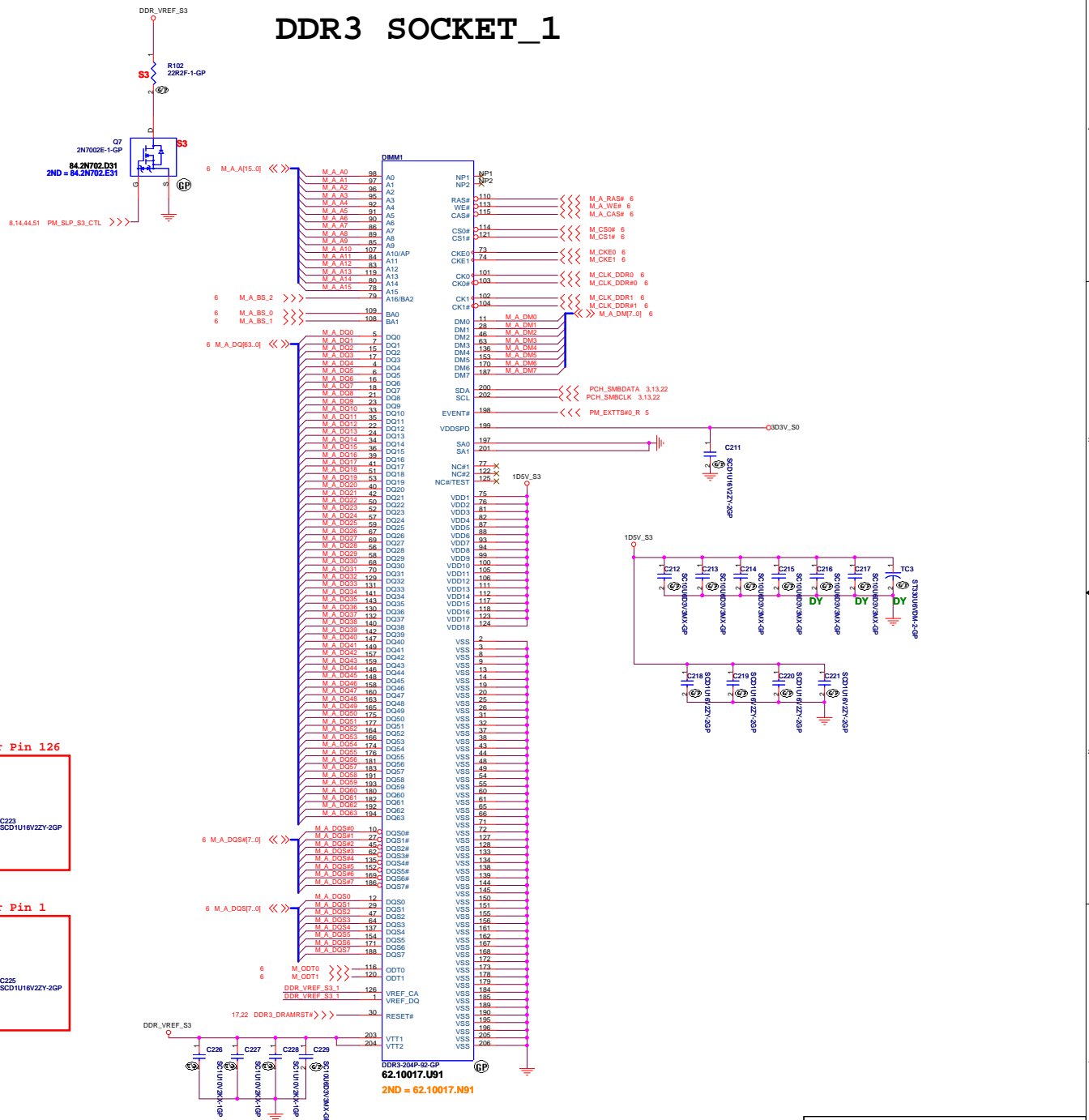
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Size	Document Number	TUCANA	
Custom		SB	
Date:	Wednesday, July 07, 2010	Sheet	19 of 56



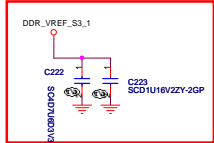
DVT 1ST

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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title PCH 9 of 9(VSS)			
Size A3	Document Number TUCANA	Rev SB	
Date: Wednesday, July 07, 2010	Sheet 20	of 56	

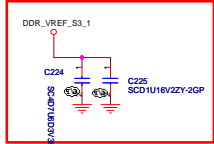
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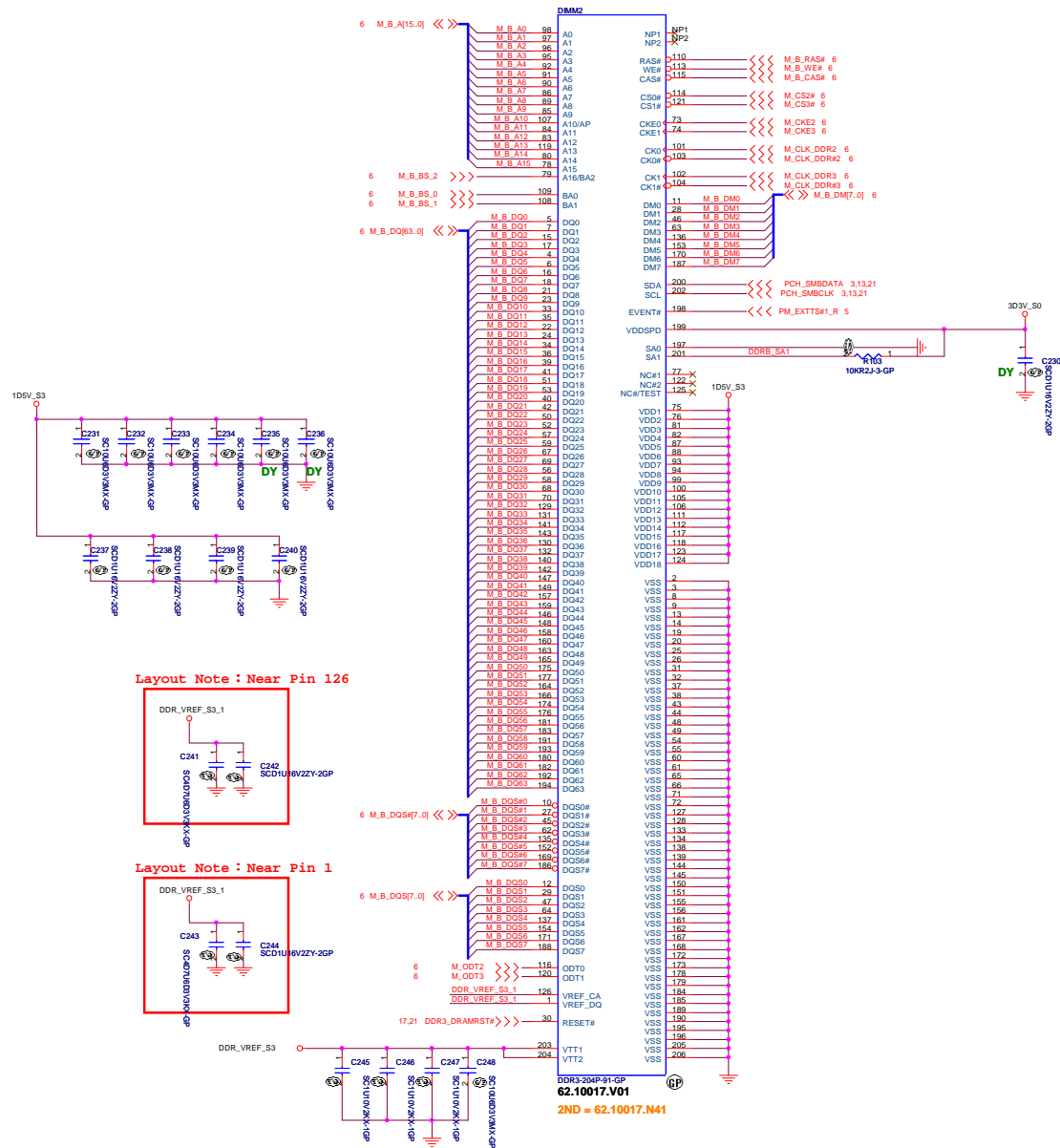
Layout Note : Near Pin 126



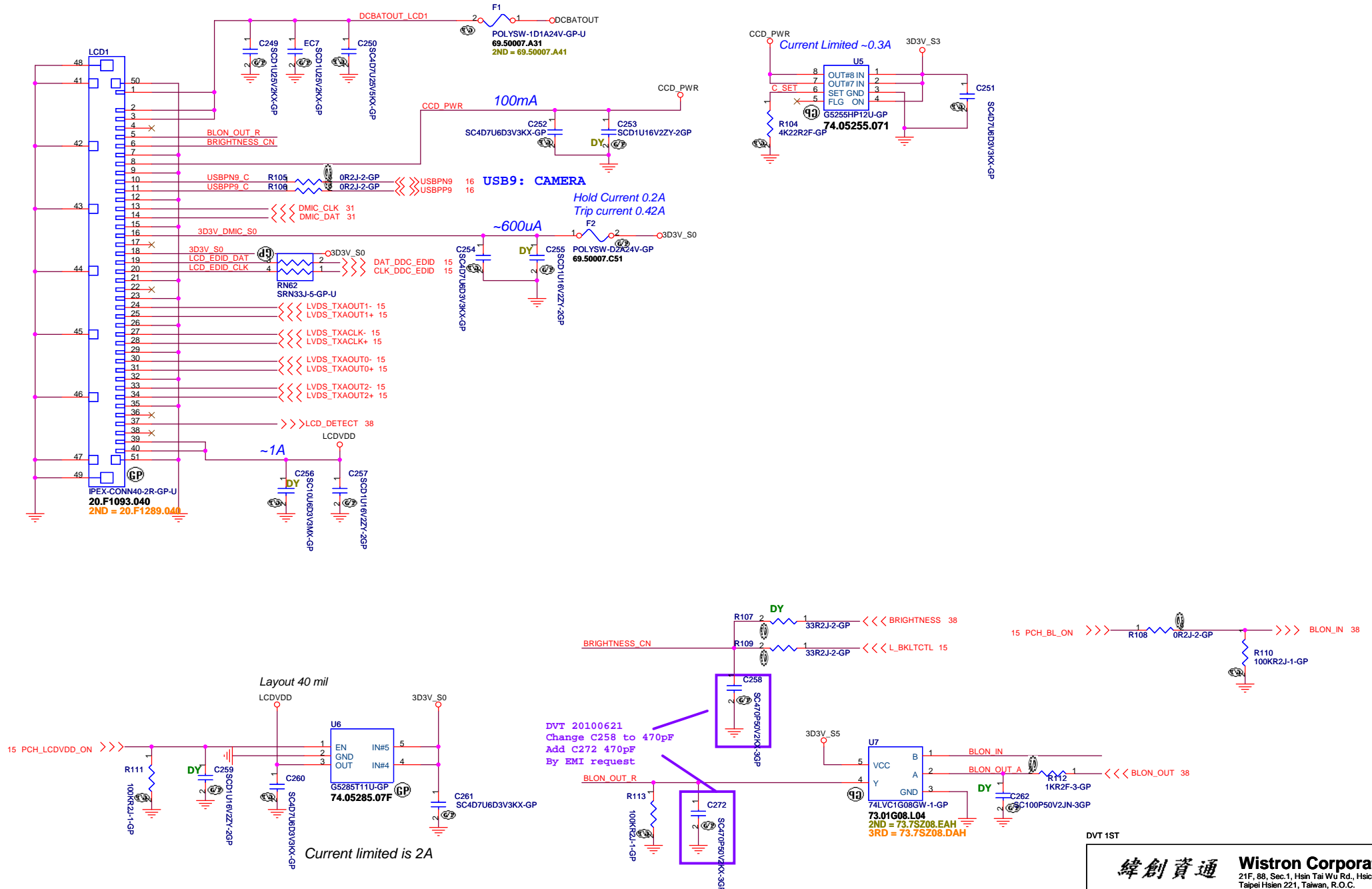
Layout Note : Near Pin 1



DDR3 SOCKET_2

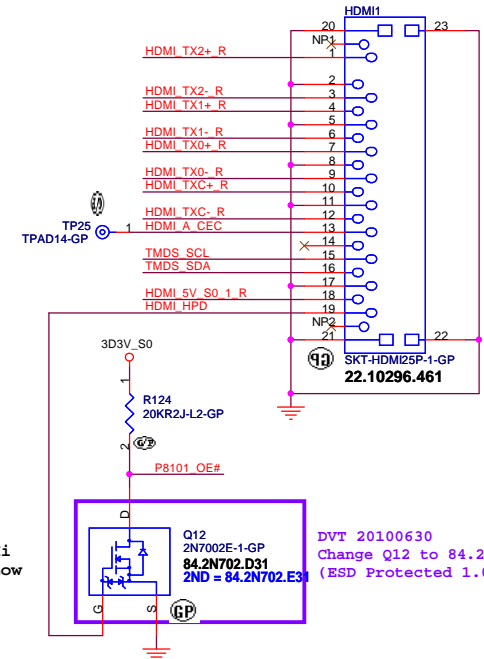
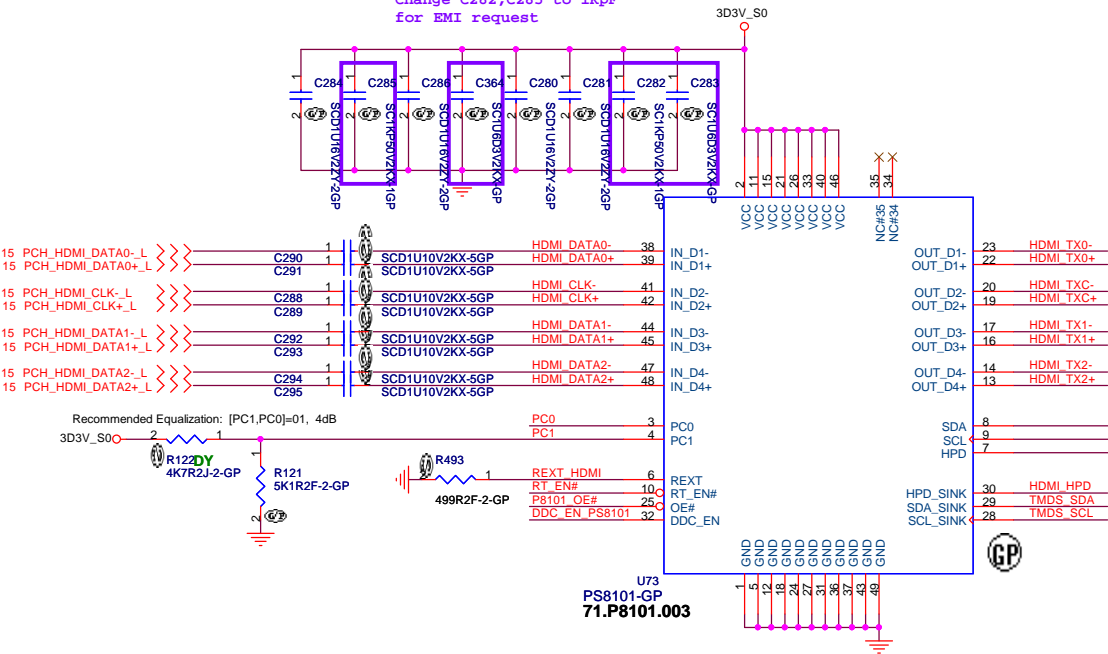


LCD/CCD CONN

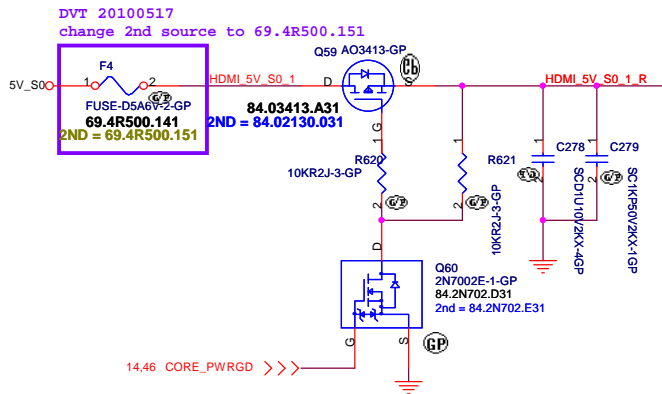


DVT 1ST

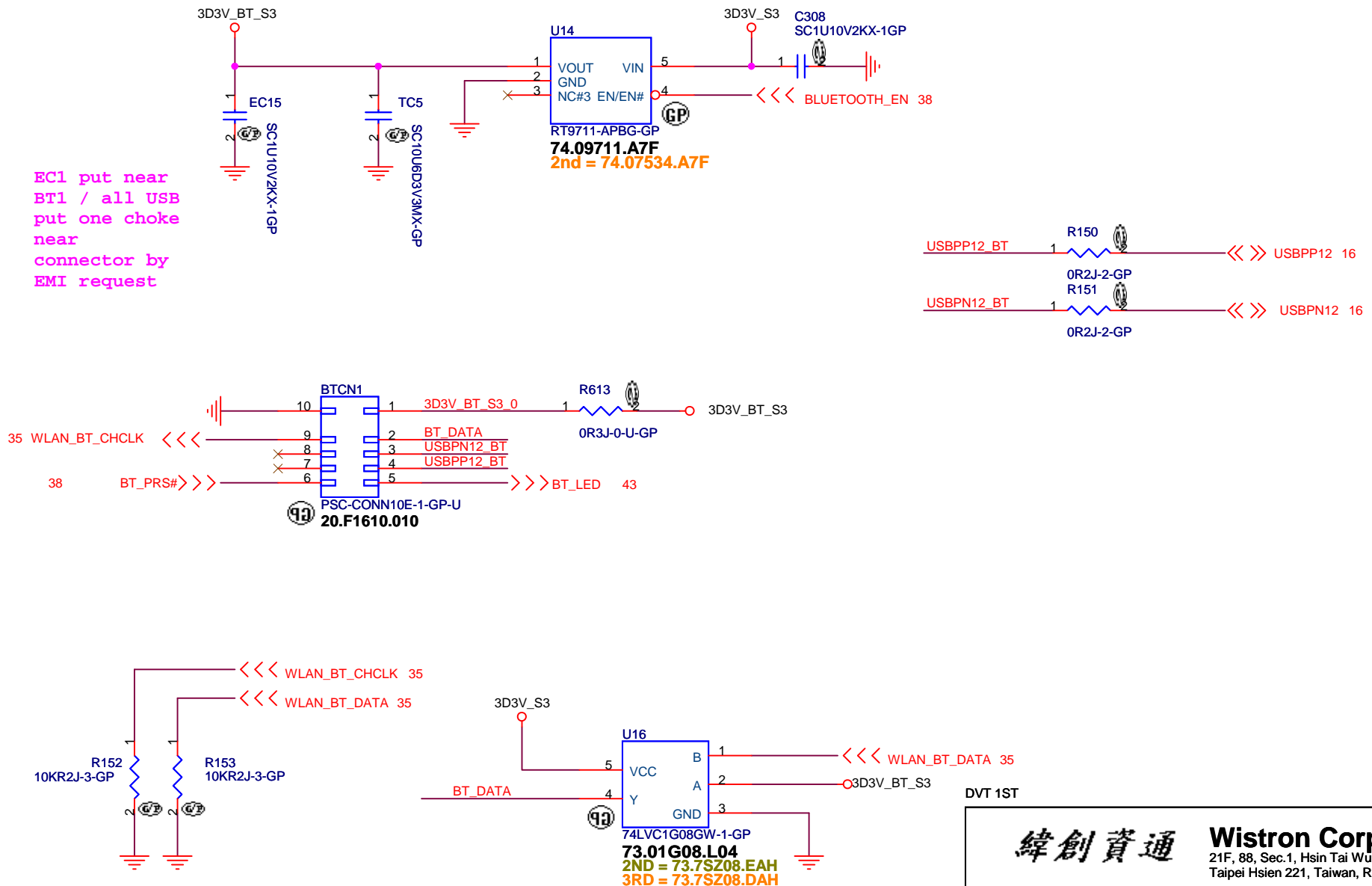
DVT 20100611
Change C283,C364 to 1uF
Change C282,C285 to 1KpF
for EMI request



HDMI in : Hi
HDMI out : Low



Bluetooth



DVT 1ST

緯創資通

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Title

Bluetooth

Size

Document Number

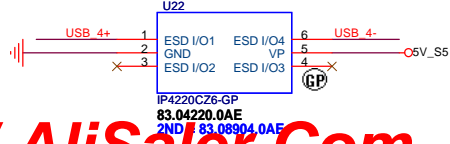
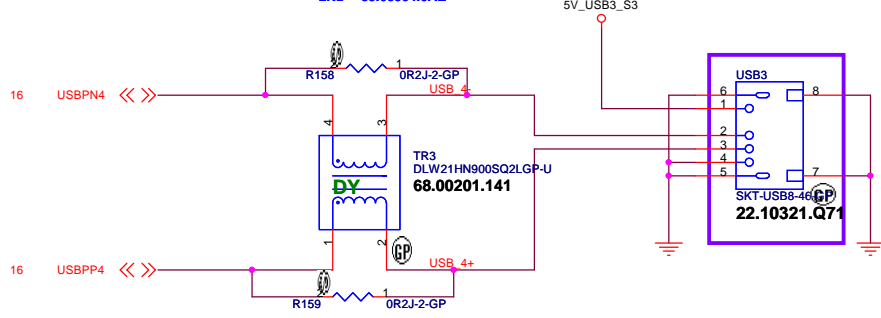
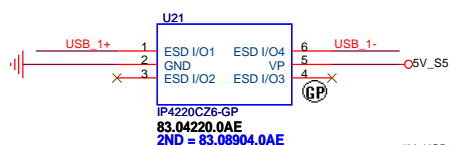
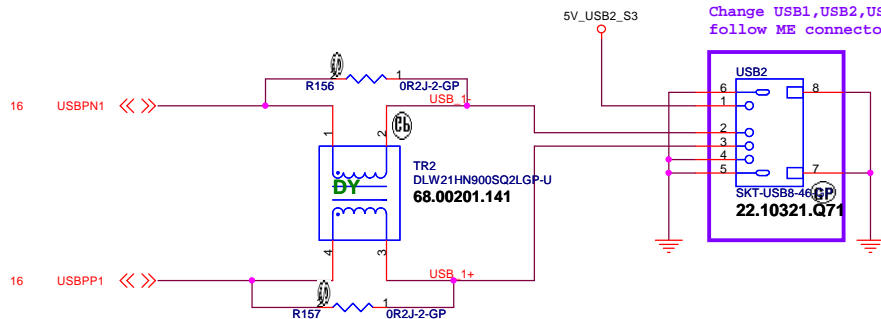
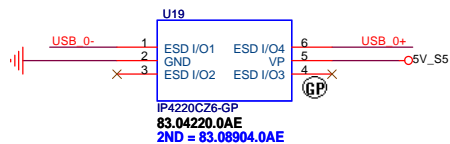
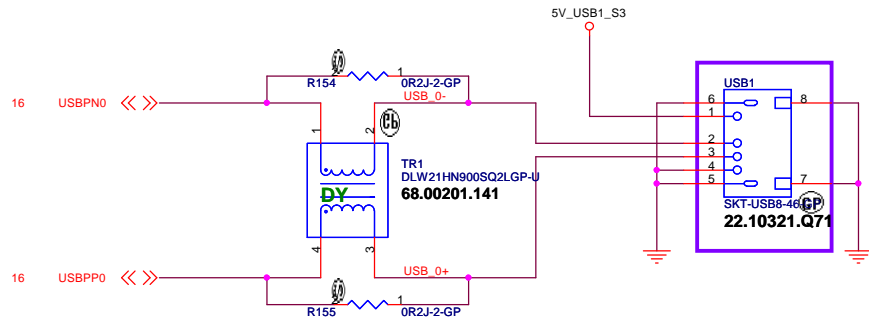
TUCANA

Rev

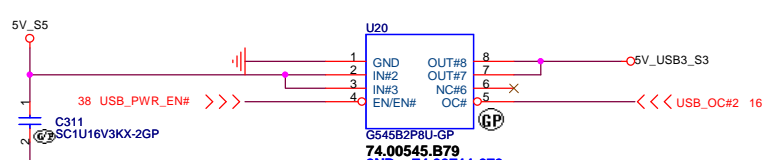
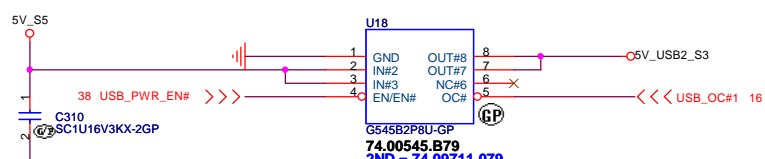
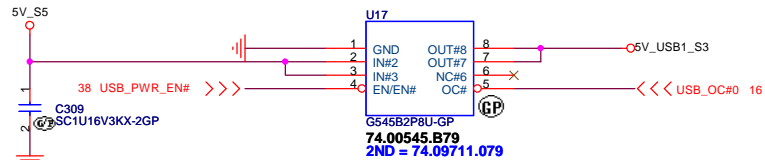
SB

Date: Wednesday, July 07, 2010

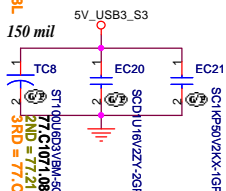
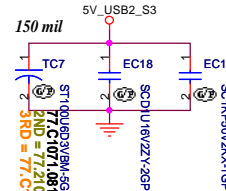
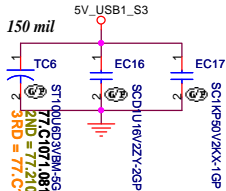
Sheet 27 of 56



DVT 20100604
Change USB1,USB2,USB3 to 22.10321.Q71
follow ME connector list.

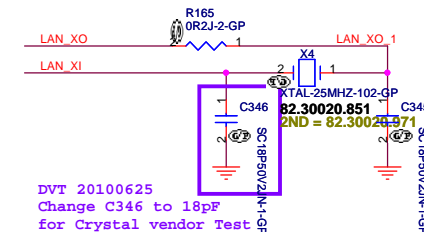
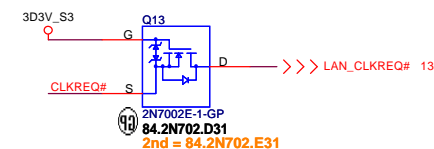
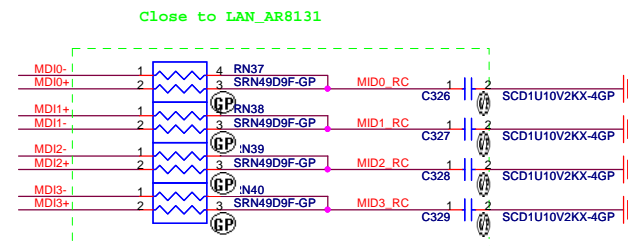
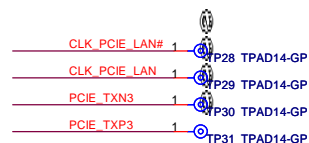
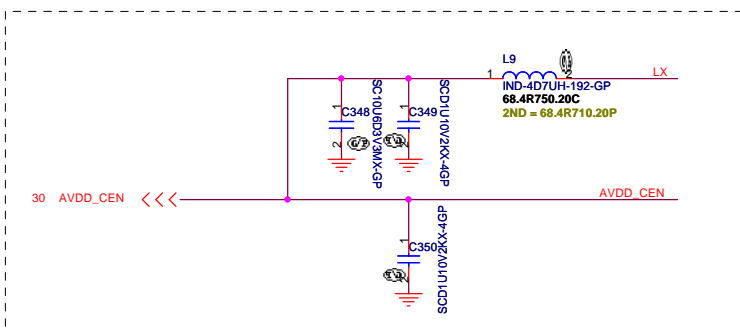
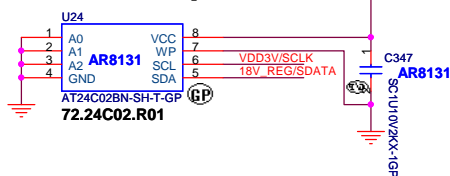
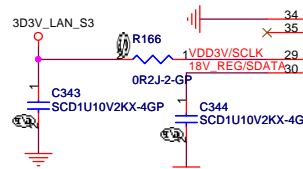
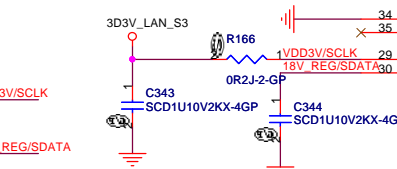
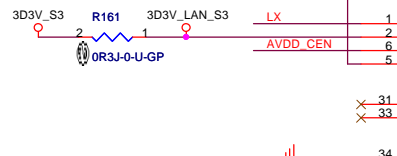
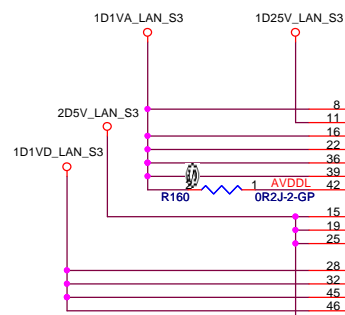
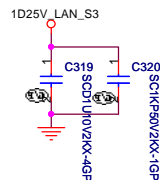


U17,U18,U20 Current Limit 1.5A



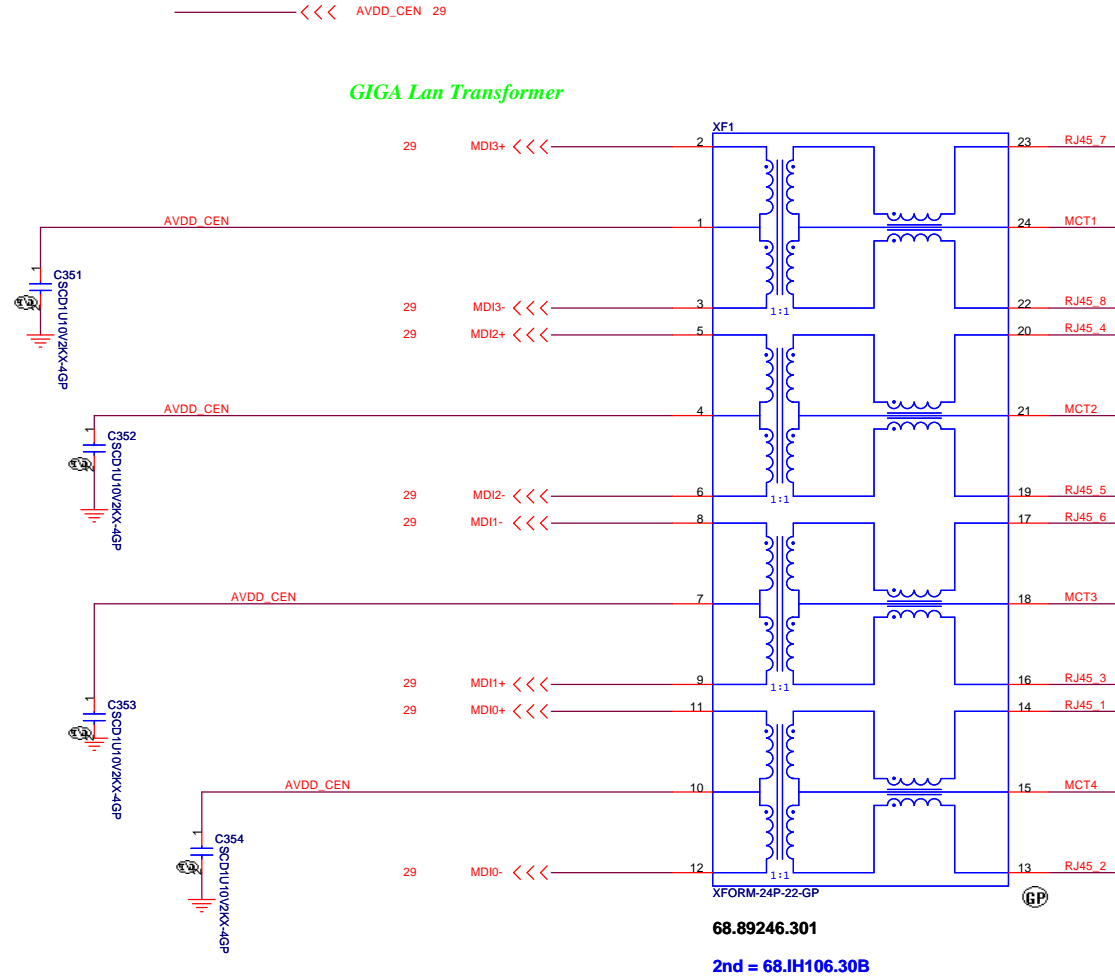
DVT 1ST

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Title: USB CONN		
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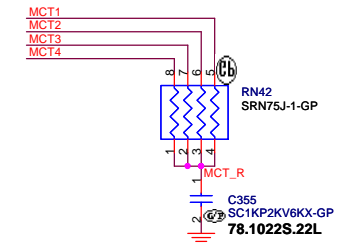
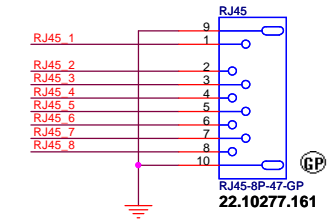


- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

LAN Transformer



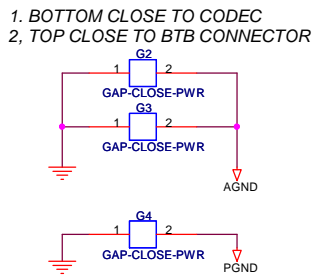
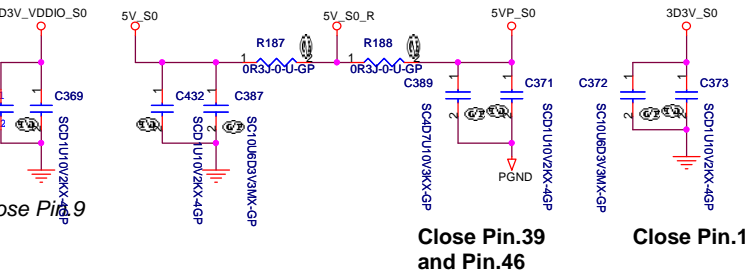
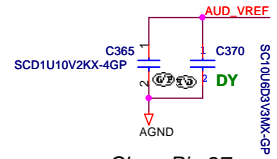
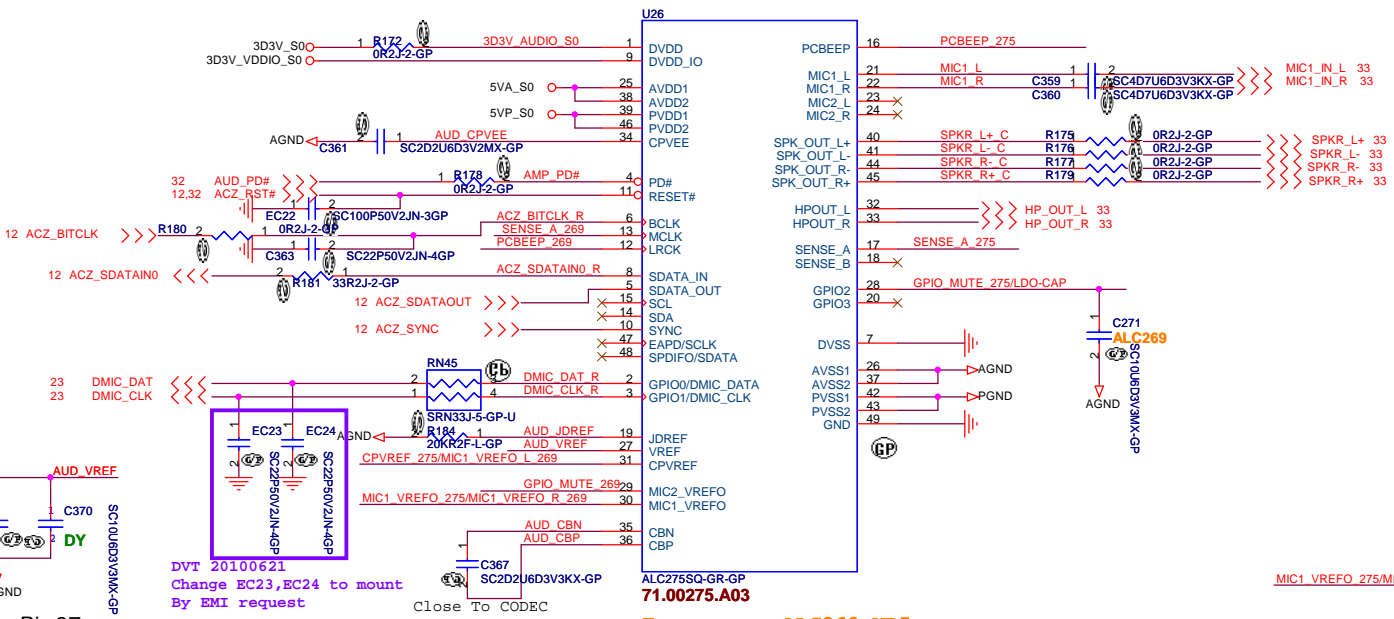
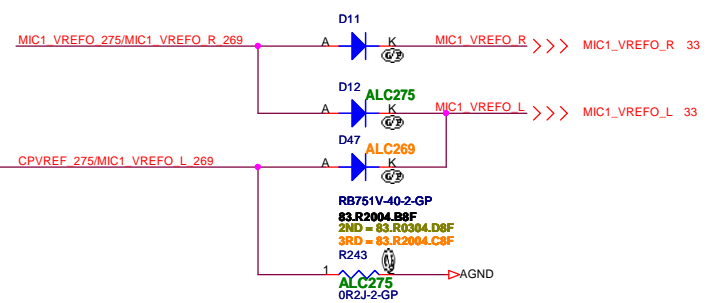
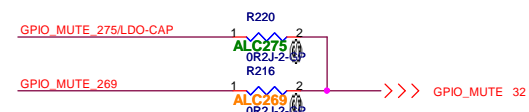
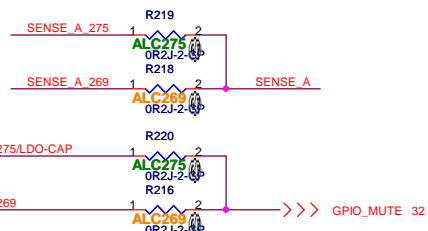
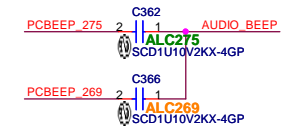
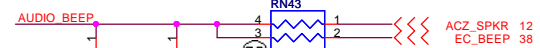
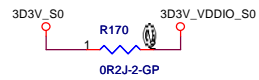
LAN Connector



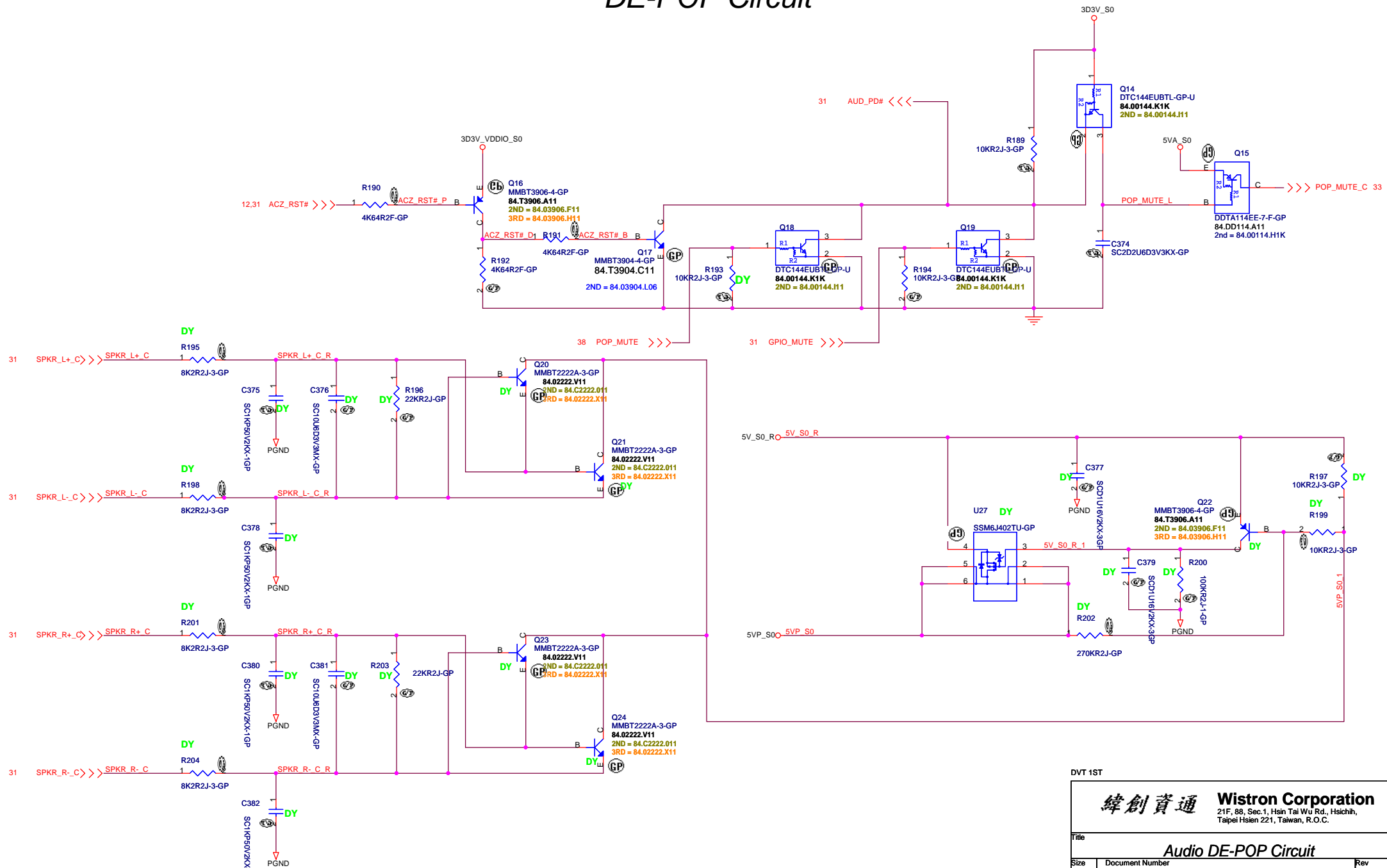
DVT 1ST

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DE-POP Circuit

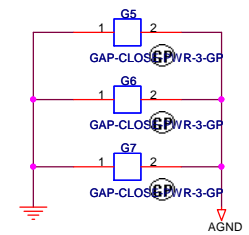
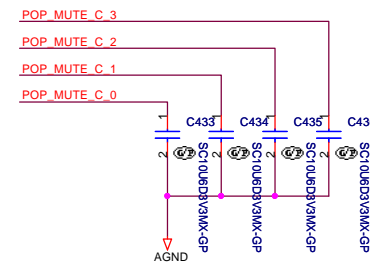
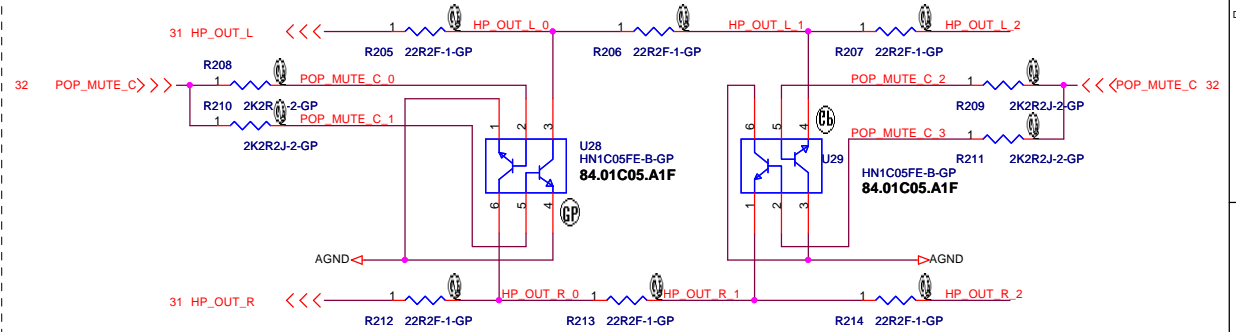
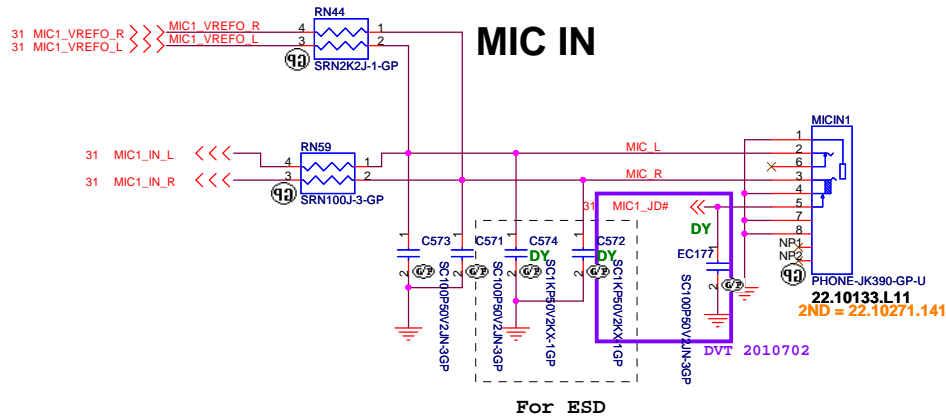
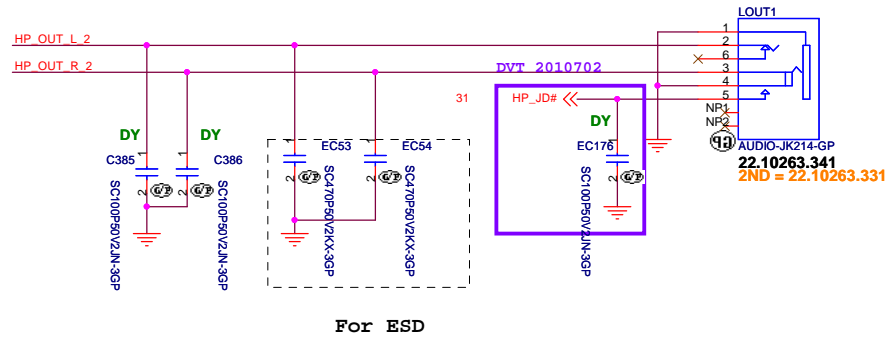


DVT 1ST

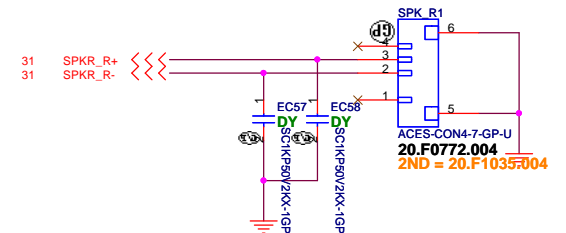
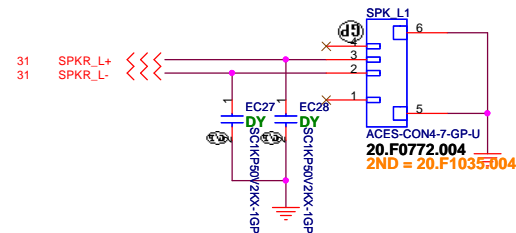
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title		Audio DE-POP Circuit	
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LINE OUT



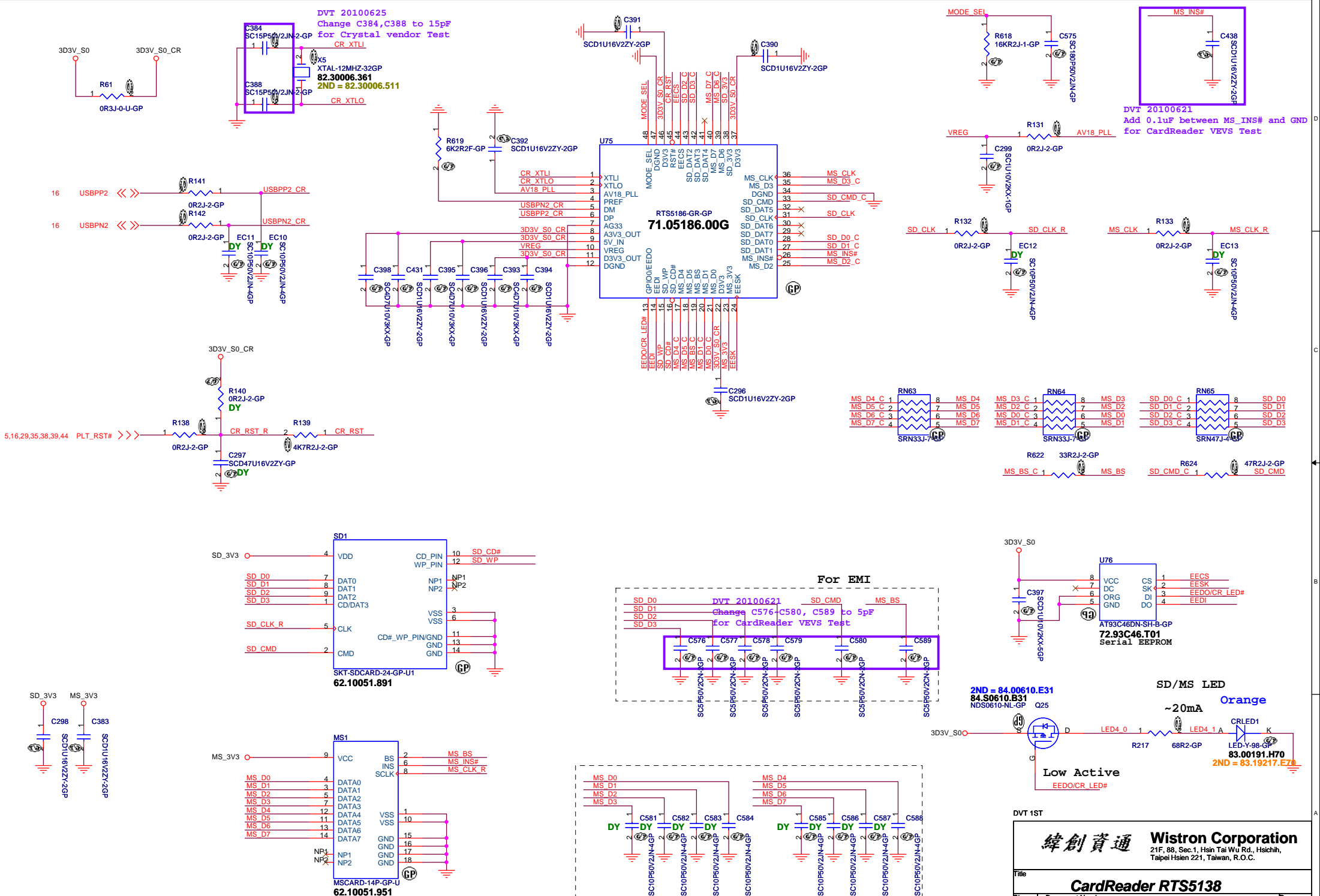
Internal Speaker CONN



DVT 1ST

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Taipei Hsien 221, Taiwan, R.O.C.

Title		
Audio Jack & Speaker		
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1

MINI1_3D3V_S3

C399 1 2 SC1U10P2KX-1GP

C400 1 2 SCD1U16V2ZY-2GP

C401 1 2 SCD1U16V2ZY-2GP

C402 1 2 SCD1U16V2ZY-2GP

C403 1 2 SCD2U16V2ZY-2GP

C404 1 2 SCD2U16V2ZY-2GP

C405 1 2 SCD2U16V2ZY-2GP

C406 1 2 SCD2U16V2ZY-2GP

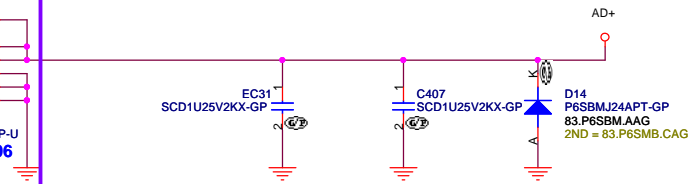
3.3V

1



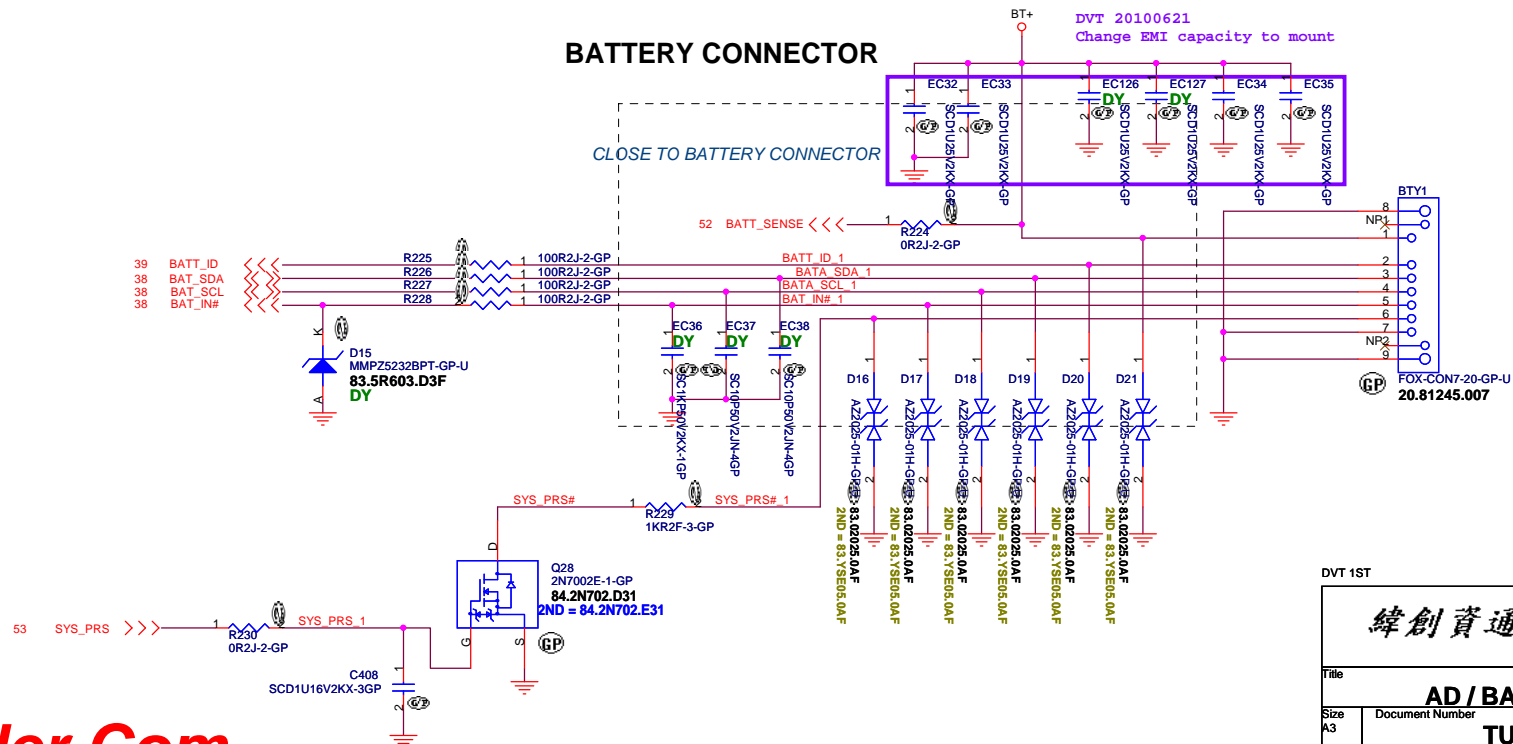
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MINI CARD CONN			
Size	Document Number		Rev
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Adaptor in to generate DCBATOUT



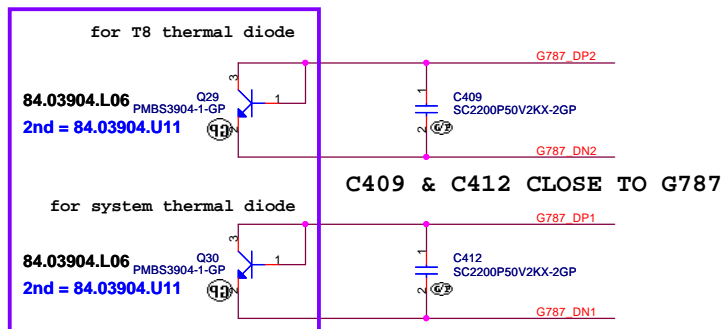
CLOSE TO BATTERY CONNECTOR

CLOSE TO BATTERY CONNECTOR

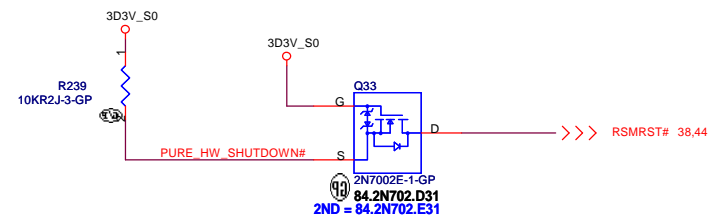
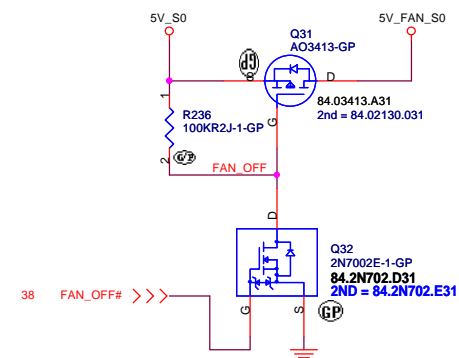
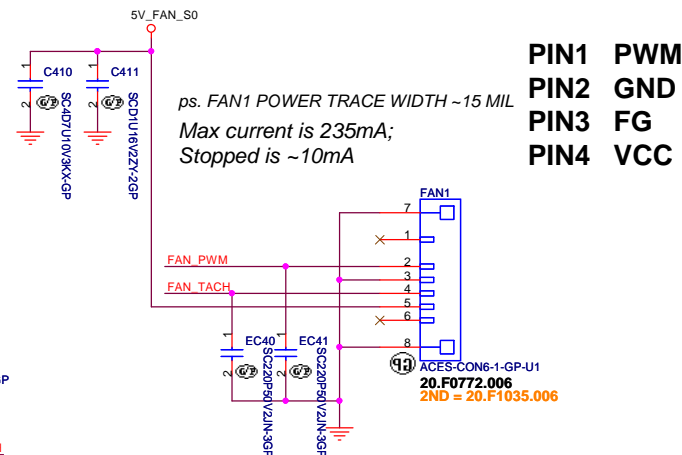
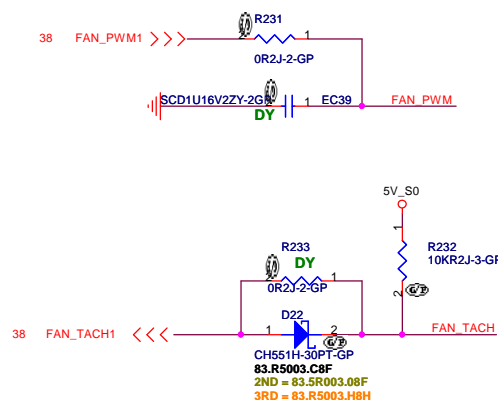
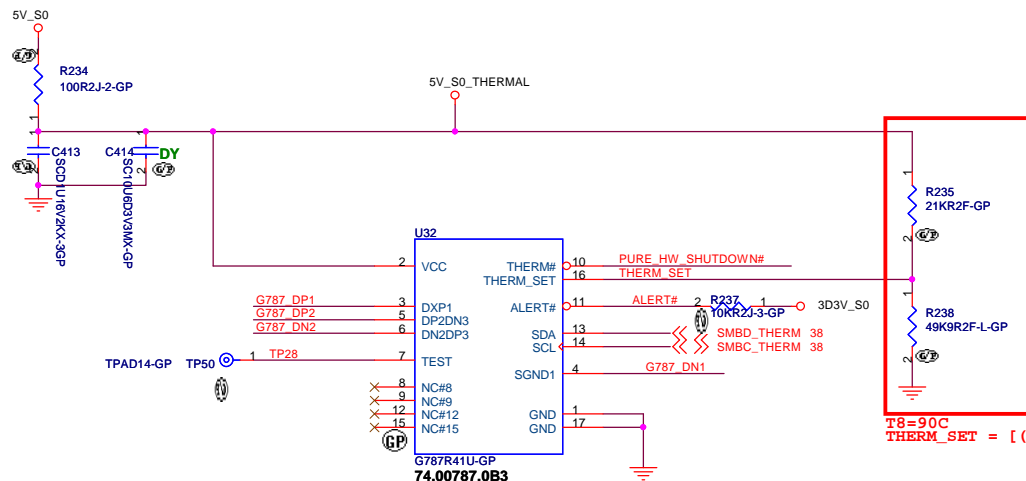


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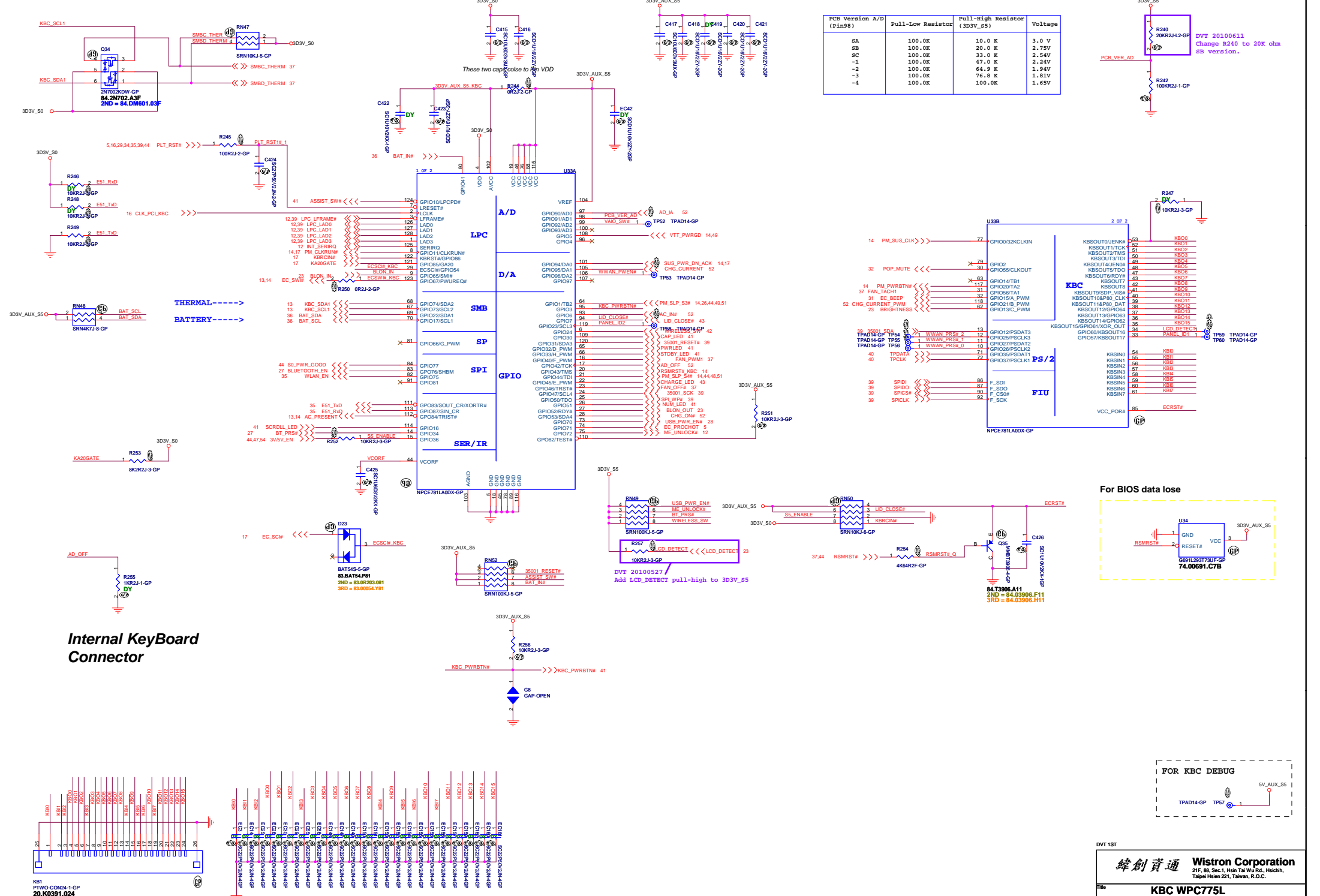
Title			
AD / BATT CONN			
Size A3	Document Number	Rev	
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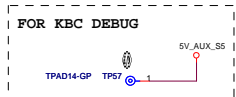
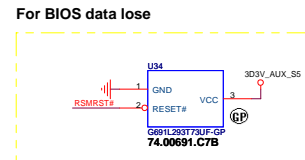
DVT 20100705
Delete Q29,Q30 main source 84.T3904.C11, follow CARAVEL-CP design



DVT 1ST



PCB Version A/D (Pin98)	Pull-Low Resistor	Pull-High Resistor (3D3V_S5)	Voltage
5A	100.0K	10.0 K	3.0 V
5B	100.0K	20.0 K	2.75V
5C	100.0K	33.0 K	2.54V
-1	100.0K	47.0 K	2.24V
-2	100.0K	64.9 K	1.94V
-3	100.0K	76.8 K	1.83V
-4	100.0K	100.0K	1.65V



Internal KeyBoard Connector

WWW.AliSaler.Com

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Rev

Size

A2

Document Number

TUCANA

Date: Thursday, July 09, 2010

Rev

SB

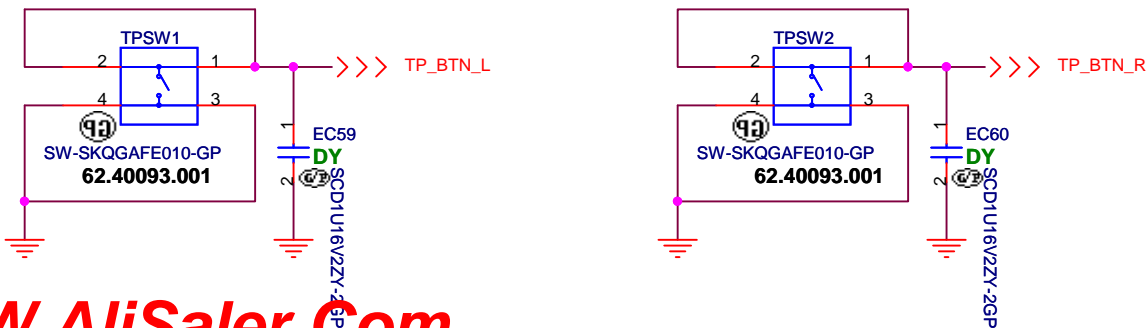
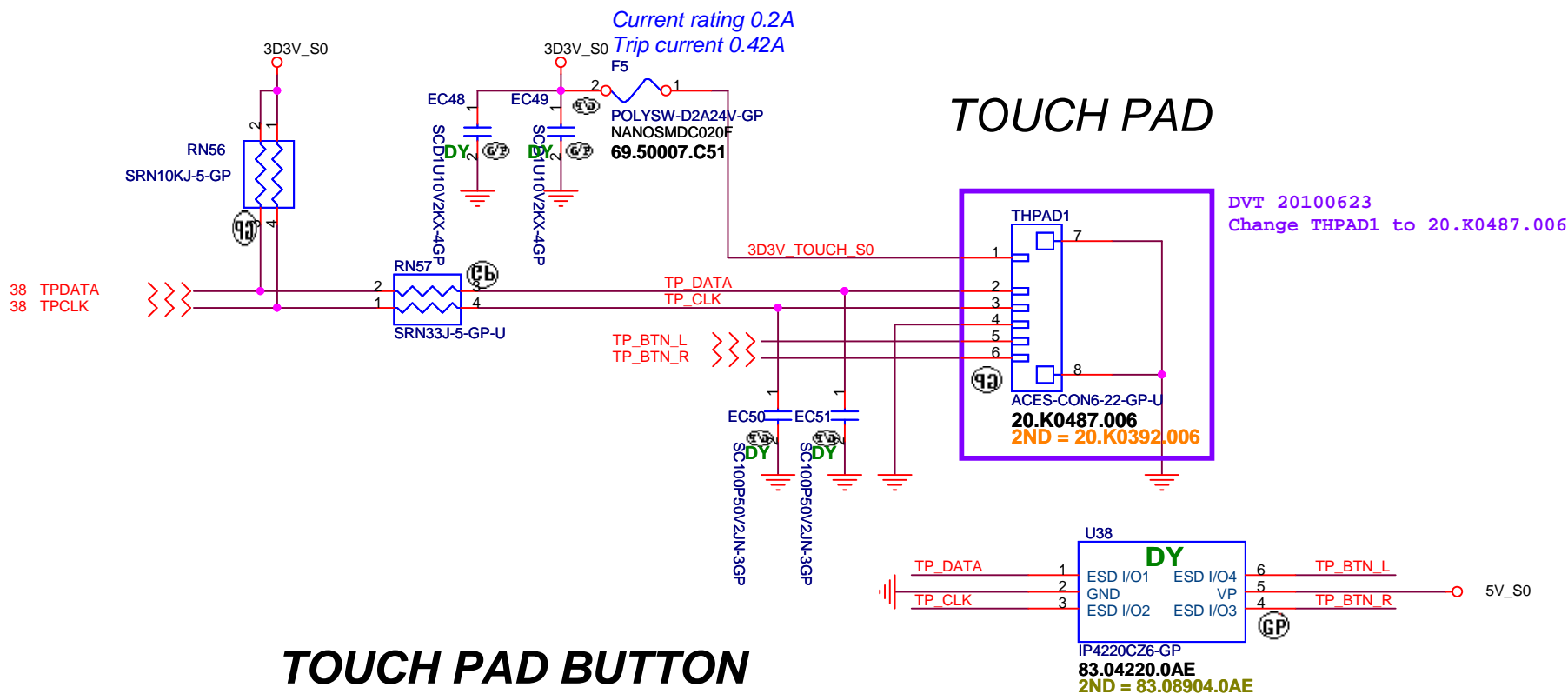
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DVT 1ST



DVT 1ST

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Taipei Hsien 221, Taiwan, R.O.C.

Title

TouchPad

Size
A4

Document Number

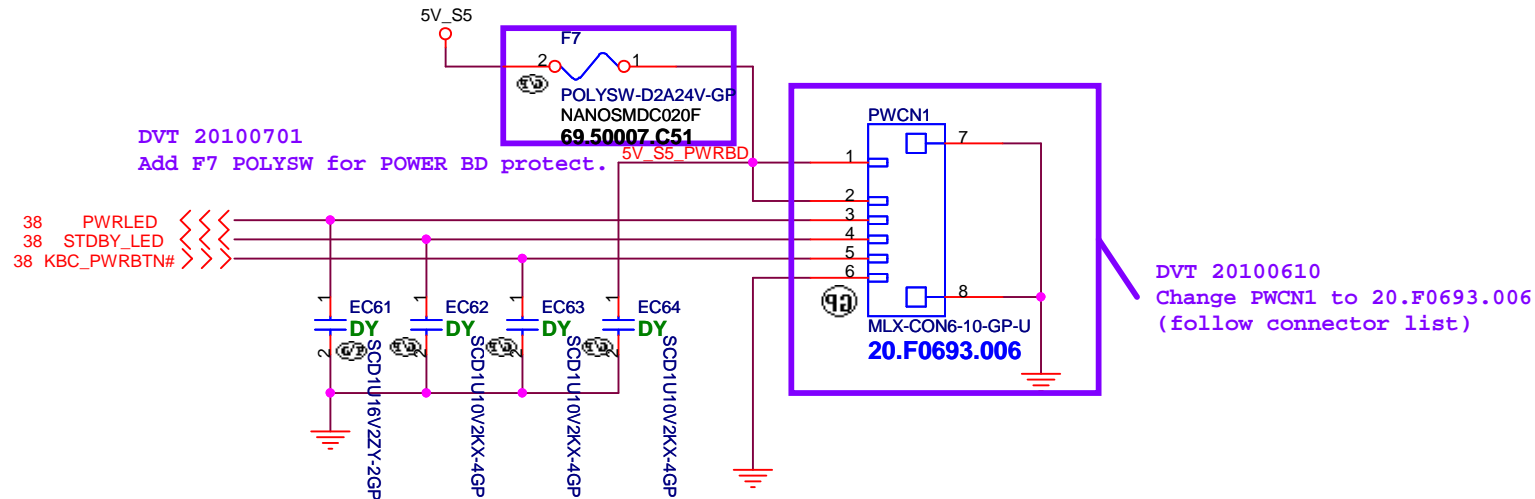
TUCANA

Rev
SB

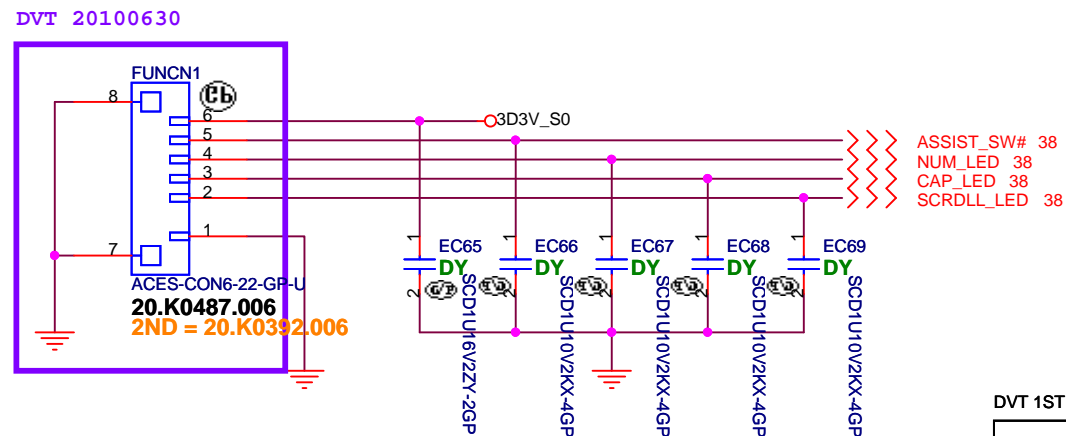
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POWER BUTTON BD CONN



FUNCTION BD CONN



DVT 1ST

緯創資通

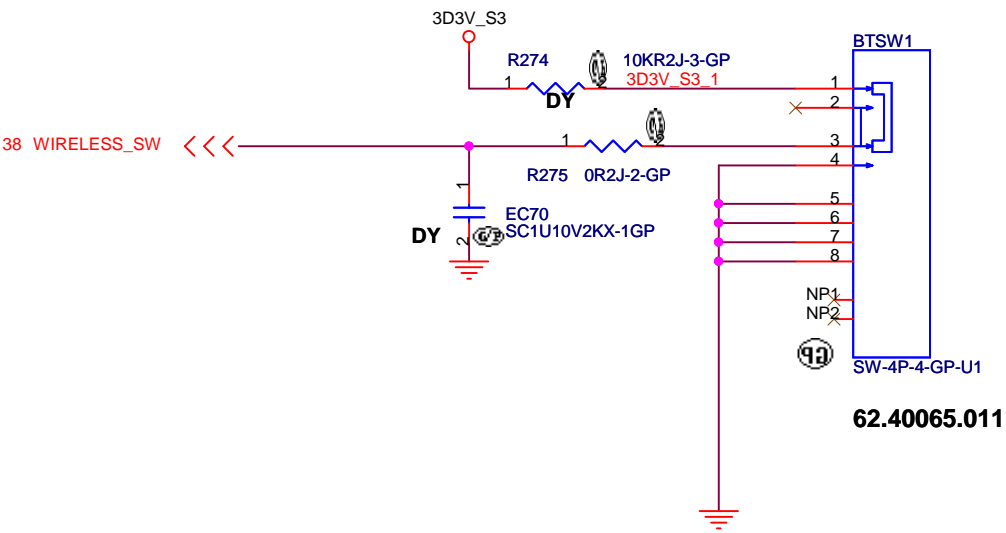
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title **FUNCTION BD & POWER BD**


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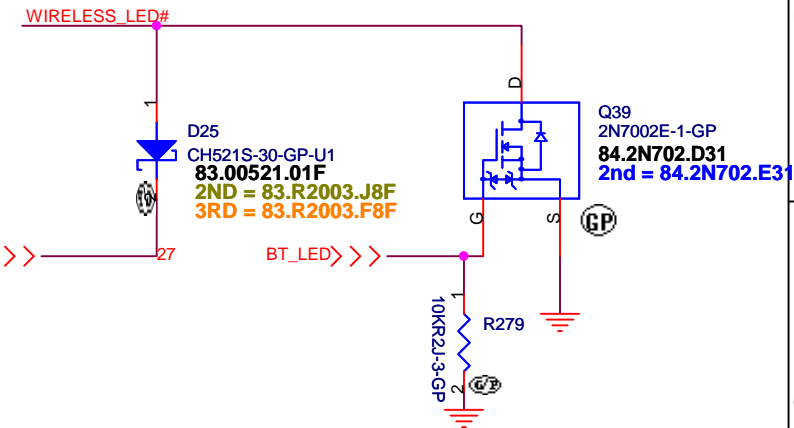
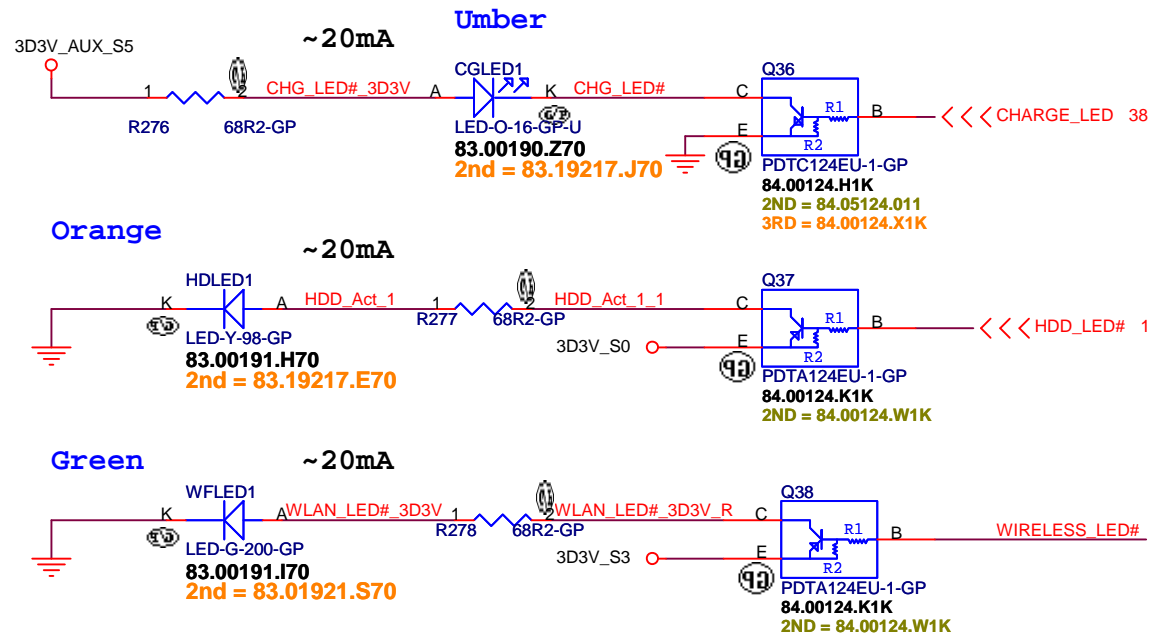
WLAN SWITCH



DVT 1ST

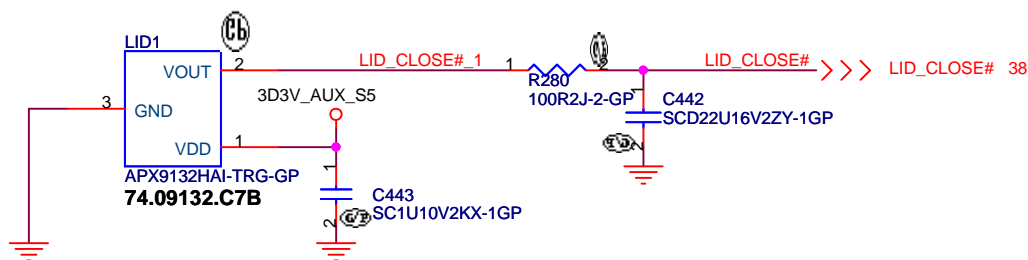
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Switch			
Size	Document Number TUCANA		Rev SB
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LED



active	High	Low
WWAN(W_DISABLE#)	ON	OFF
WLAN(WLAN_LED#)	OFF	ON
Bluetooth(BT_LED)	ON	OFF

Cover Up Switch



Common wireless SW(mechanical)	ON							
WLAN SW(software)	ON	OFF	ON	OFF	ON	OFF	ON	OFF
WWAN SW(software)	ON	ON	OFF	OFF	ON	ON	OFF	OFF
Bluetooth SW(software)	ON	ON	ON	ON	OFF	OFF	OFF	OFF
LED	TURN ON							OFF

DVT 1ST

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Lid Switch & LED

Size

Document Number

TUCANA

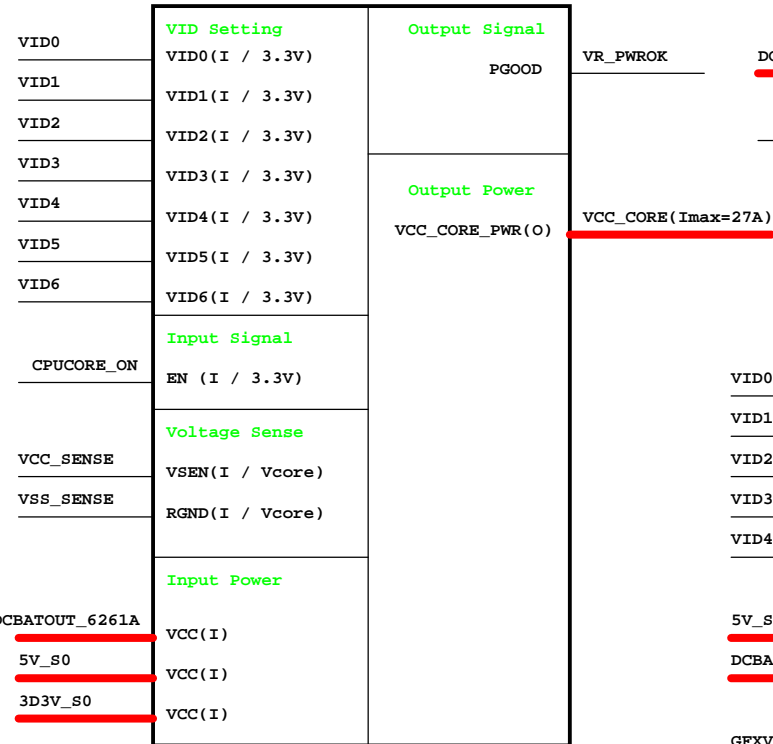
Rev

SB

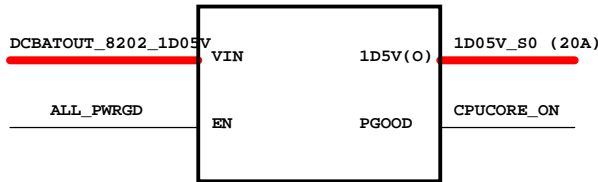
Date: Wednesday, July 07, 2010

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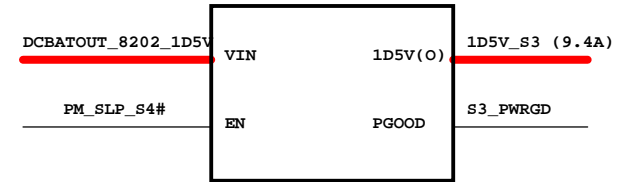
CPU_CORE
ADP3211



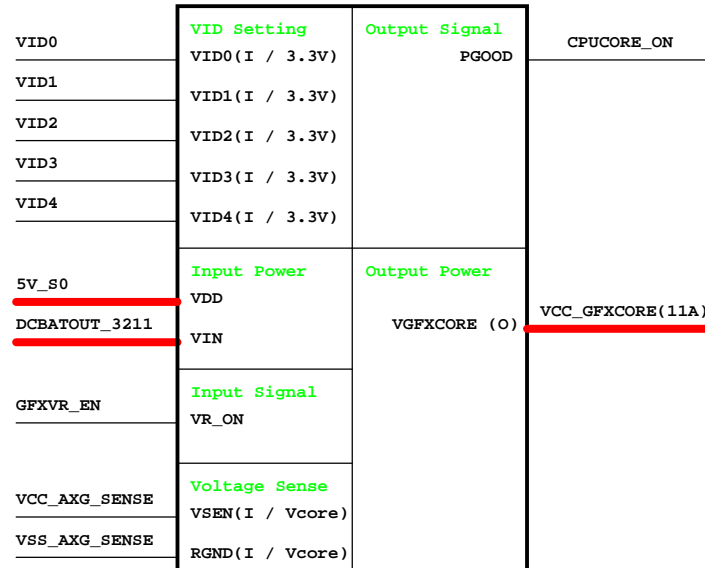
RT8209 1D05V_S0



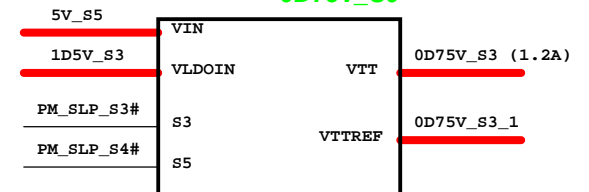
RT8209 1D5V_S3



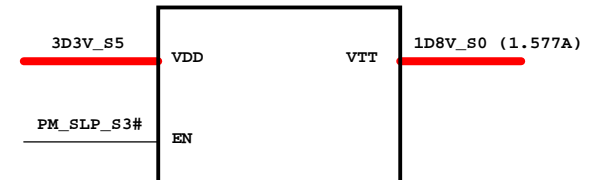
GFX_CORE/ VGA_CORE
ADP3211



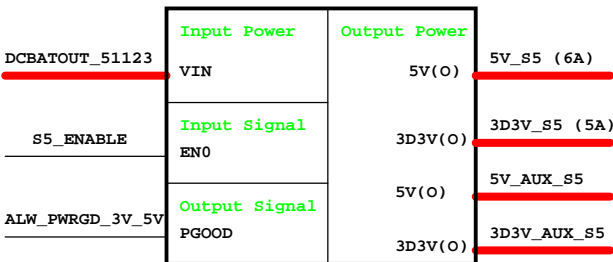
RT9026 0D75V_S0



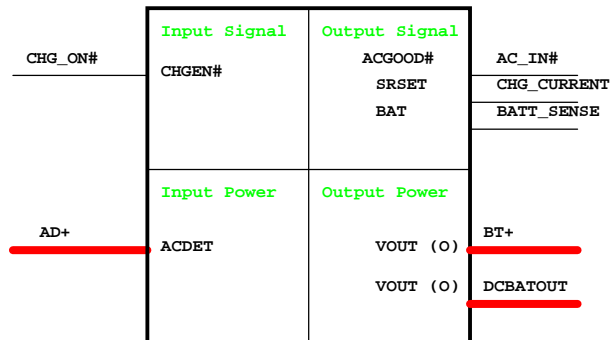
RT8015 1D8V_S0



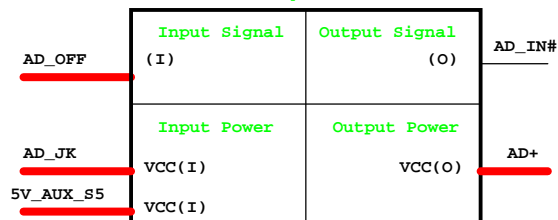
5V/3D3V
RT8223



Charger BQ24751

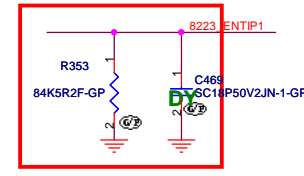
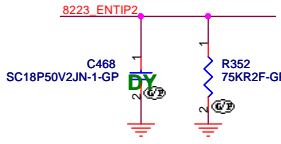
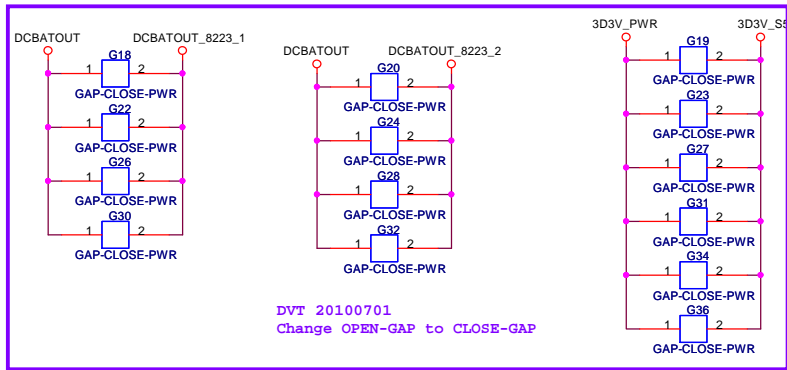


Adapter



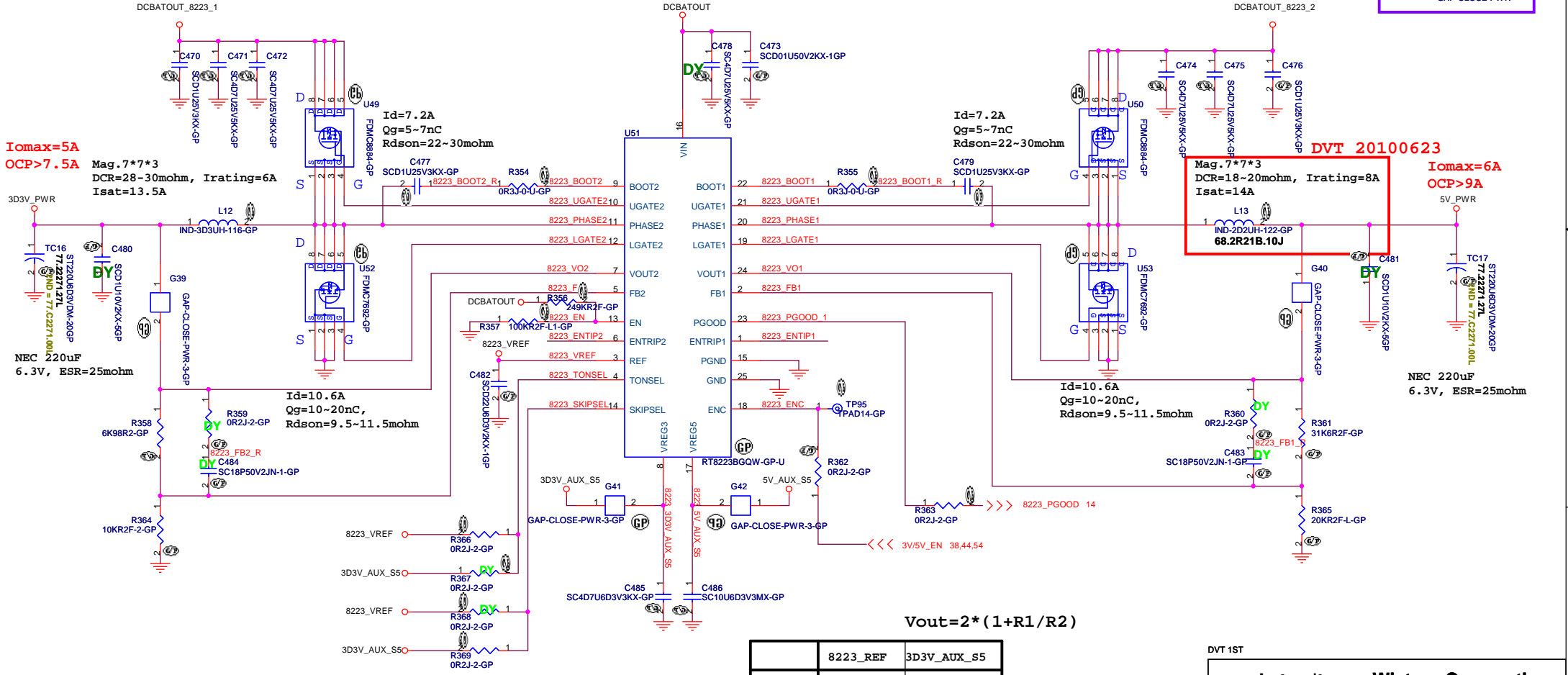
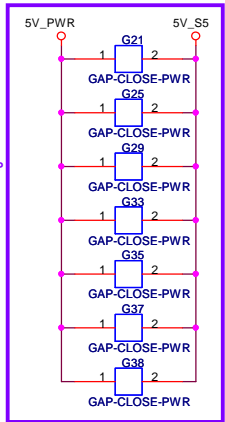
DVT 1ST





DVT 20100623

DVT 20100701
Change OPEN-GAP
to CLOSE-GAP



	8223_REF	3D3V_AUX_S5
SKIPSEL	PWM	00A AUTOSKIP
TONSEL	245k/CH1 305k/CH2	300k/CH1 375k/CH2

5V_S5

GAP-CLOSE-PWR

TC28

SC1U10V2KX-1GP

C487

R370

2D2R3-1-U-GP

1D5 V5FILT

C491

SC1U10V2KX-1GP

R371

0R33-0-U-GP

8209 1D5_PHASE 1

C492

SCD1U25V3KX-GP

R372

0R33-0-U-GP

Id=14.3A

Qg=9.2~14nC

Rdson=11~14mohm

8209 1D5_UGATE R

U54

SI7686DP-T1-GE3-GP

84.07686.A37

Mag. 1.0uH

DCR=2.9~3.3mohm

I_{dc}=18A, I_{sat}=36A

I_{omax}=9.4A

OCP>14.1A

1D5V_PWR

L14

IND-1UH-33-GP

68.1R01B.10J

20100401

31K6R2F-GP

R375

8209 1D5_FB

C493

SC33F50V21N36P

C494

TC18

ST330U2D5VBM-1-GP

80.3371V.A2L

2ND=77.23371.371L

Panasonic 220uF

2V, ESR=9mohm

14,38,44,51 PM_SLP_S4# >>>

R374

0R2J-2-GP

R376

100KR2F-L1-GP

C495

SCD1U10V2KX-5GP

R373

249KR2F-GP

8209 1D5_EN

8209 1D5_TON

8209 1D5_CS

U55

VDD

VDDP

FB

BOOT

PHASE

VOUT

PGOOD

GND

PGND

NC#15

EN/IDEM

TON

CS

RT8209EGQW-GP

3D3V_S0

R378

10KR2F-2-GP

R379

0R2J-2-GP

ALL_PWRGD

44,49,51

20100331

Id=19.4A

Qg=16.8~25.5nC,

Rdson=4.9~6.1mohm

20100331

V_{out}=0.75*(1+R1/R2)

DVT 20100623

15D5V_PWR

15D5V_S3

G43 1 2

GAP-CLOSE-PWR

G44 1 2

GAP-CLOSE-PWR

G45 1 2

GAP-CLOSE-PWR

G46 1 2

GAP-CLOSE-PWR

G48 1 2

GAP-CLOSE-PWR

G50 1 2

GAP-CLOSE-PWR

G52 1 2

GAP-CLOSE-PWR

G54 1 2

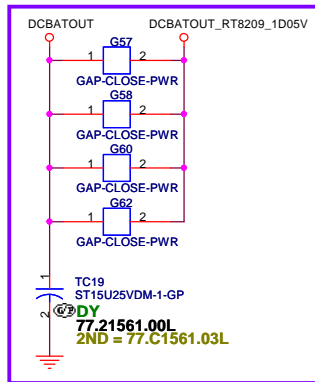
GAP-CLOSE-PWR

G55 1 2

GAP-CLOSE-PWR

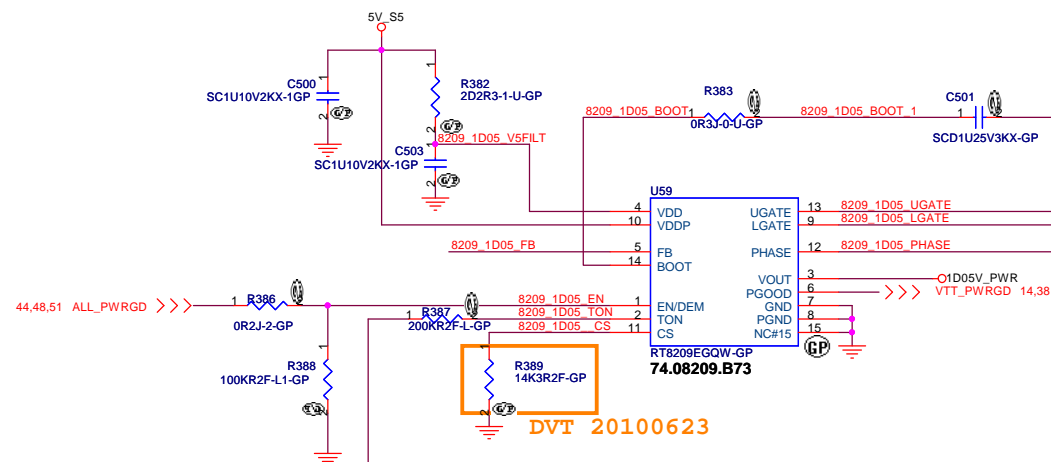
G56 1 2

GAP-CLOSE-PWR

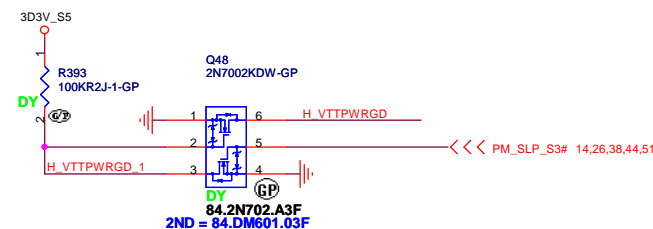


DVT 20100701
Change OPEN-GAP to
CLOSE-GAP

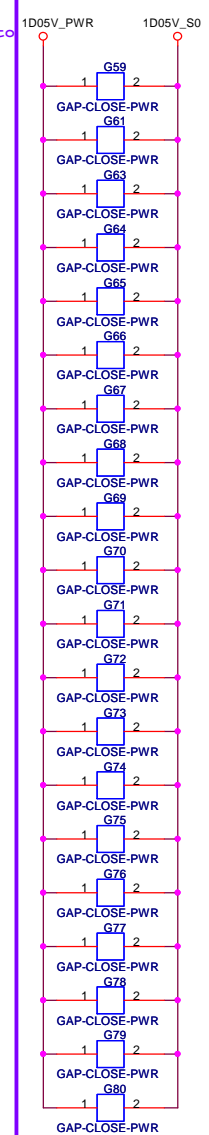
RT8209 1D05V



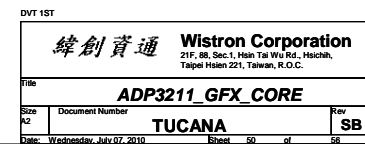
The processor needs to be warned about the VTT rails shutdown at least 100 ns before the VTT rail falls to -5% of nominal value.



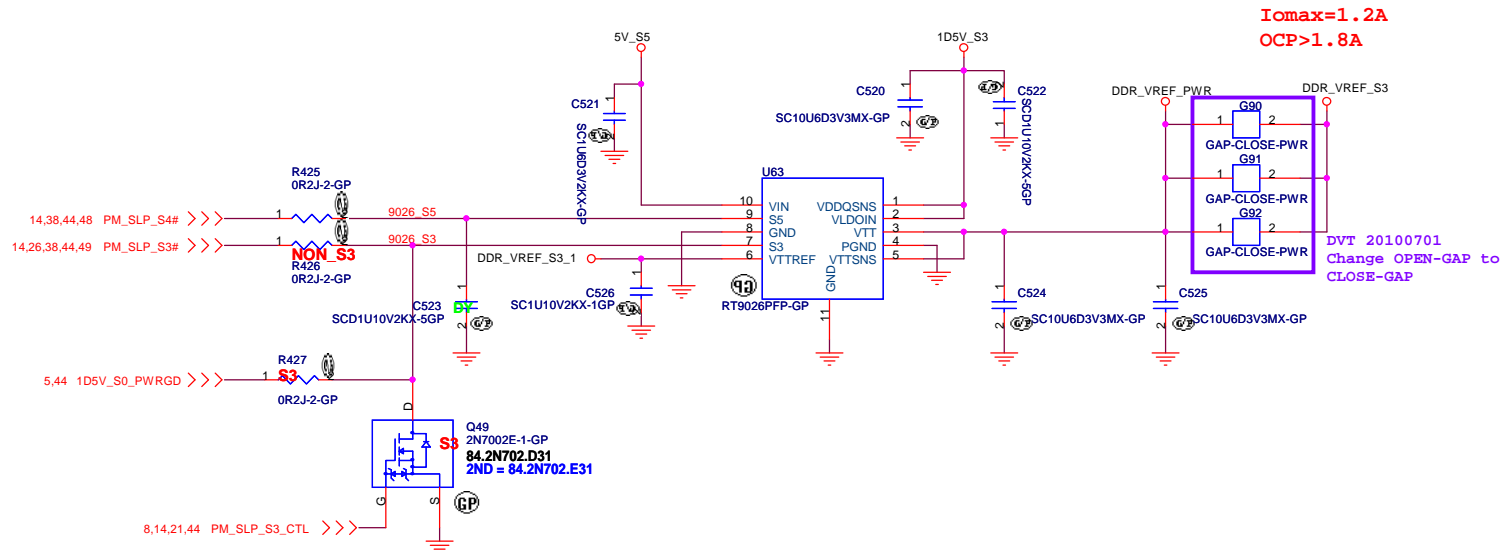
DVT 20100701
Change OPEN-GAP to
CLOSE-GAP



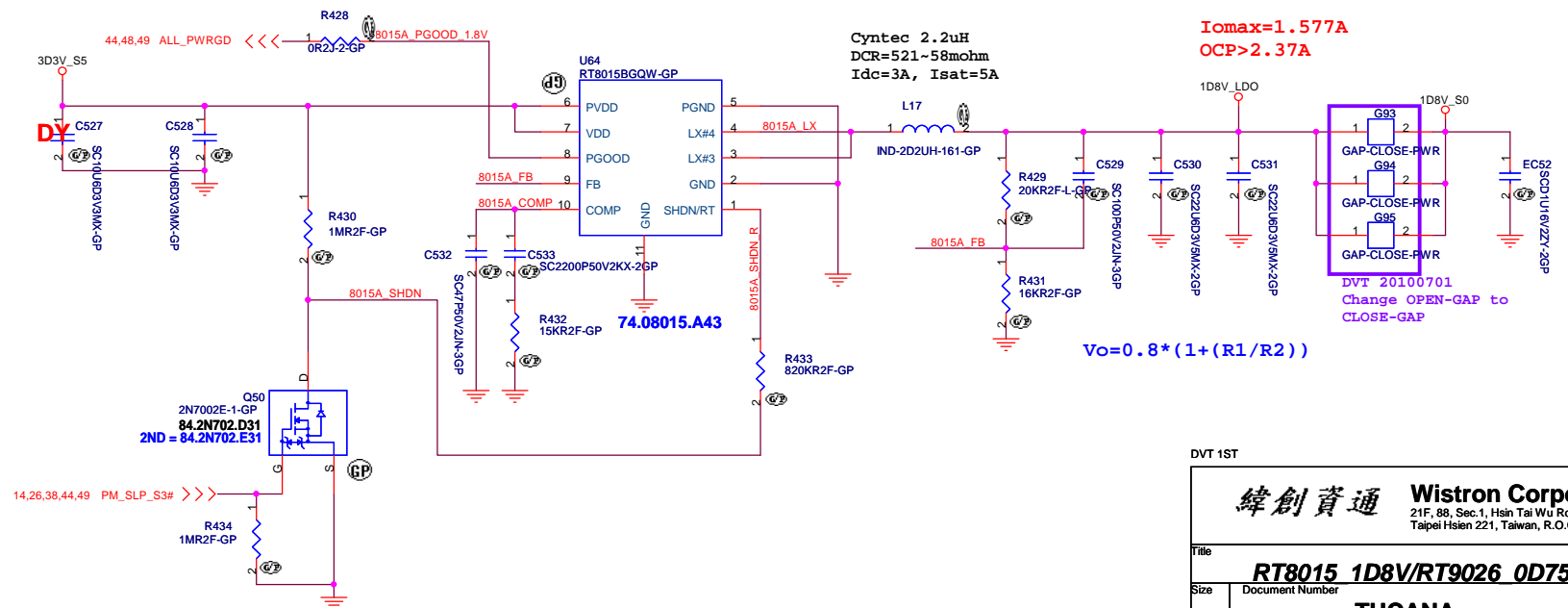
DVT 1ST



RT9026 for 0D75V_S3



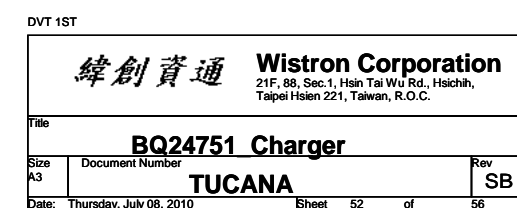
RT8015 for 1D8V_S0

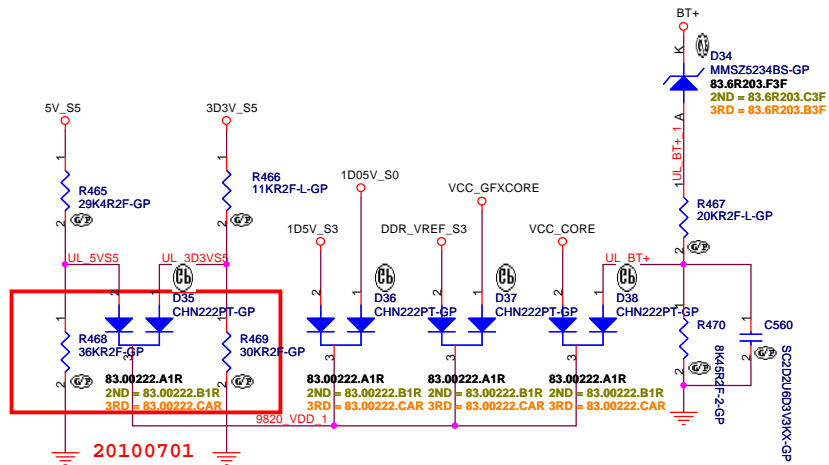


DVT 1ST

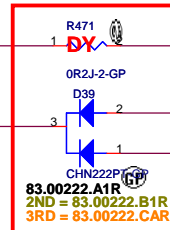
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
RT8015 1D8V/RT9026 0D75			
Size	Document Number		Rev
	TUCANA		SB
Date:	Wednesday, July 07, 2010	Sheet 51 of	56



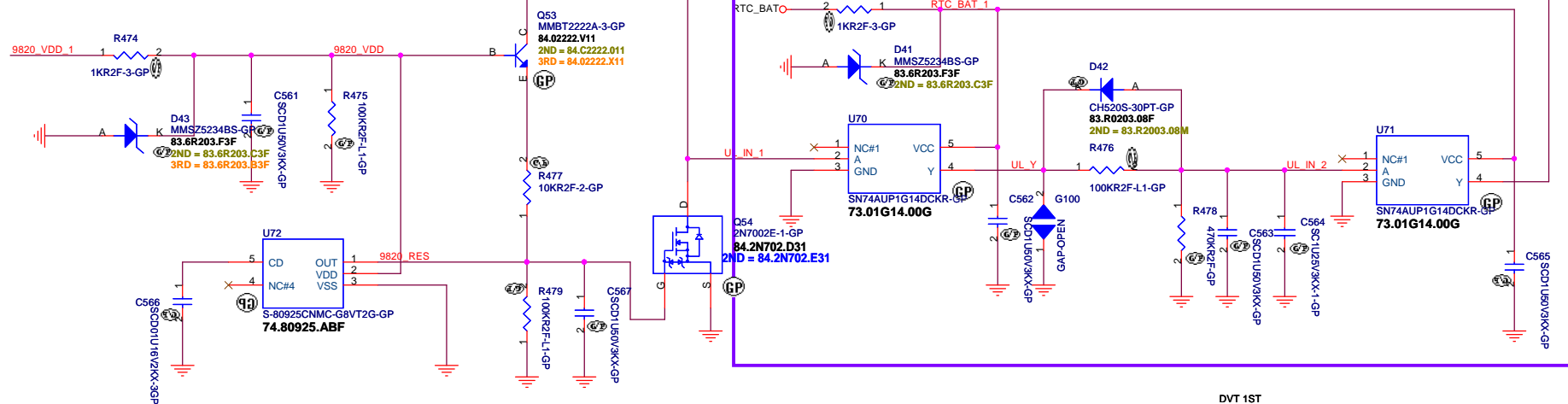
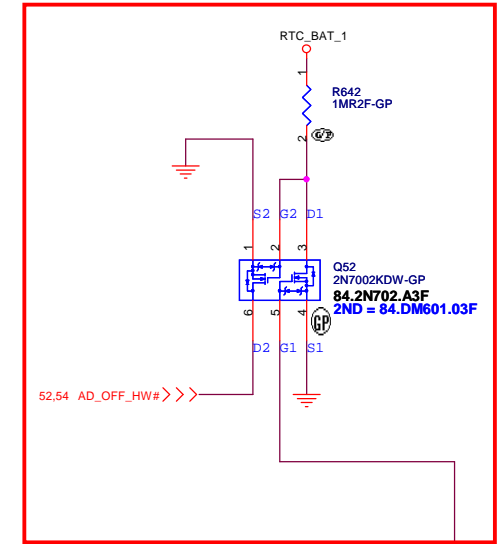


20100701



DVT 20100701
Power Team modify

20100706



DVT 1ST

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			UL circuit
Size	Document Number	Rev	
A3	TUCANA	SB	
Date:	Wednesday, July 07, 2010	Sheet	53 of 56

EVT

2010/5/17	P.52[BQ24751_Charger]	Del D31 2nd 3rd source	2010/7/2	P.38[KBC_NPCE781L / KB]	Rename H_PROCHOT# to EC_PROCHOT
2010/5/17	P.25[HDMI CONN_PS8101]	Change 2nd source to 69.4R500.151		P.5[CPU SFF(2 of 8)-CLK/Thermal]	Add R128 for EC_PROCHOT pull-low to Gnd
2010/5/24	P.26[HDD Connector]	Change R148 to 3.3K ohm ,add C437 for PM_SLP_S3# Delay		P.5[CPU SFF(2 of 8)-CLK/Thermal]	Add Q61 for EC_PROCHOT to PROCHOT#
2010/5/27	P.38[KBC_NPCE781L / KB]	Add LCD_DETECT pull-high to 3D3V_S5		P.33[Audio Jack]	Add EC176 for HP_JD# to GND , Set Dummy for ESD.
2010/5/31	P.52[BQ24751_Charger]	Mount C546,R451,R449,Q51 for battery can't Changer			Add EC177 for MIC1_JD# to GND , Set Dummy for ESD.
2010/6/1	P.24[CRT CONN]	Change F6 to 69.44002.001, for Cadiz use		P.55[EMI/Spring/Boss]	Change SPR1 to 34.42T14.002
	P.33[Audio Jack]	Change MICIN1 to 20.10133.L11 , follow connector list			
	P.28[USB]	Change USB1,USB2,USB3 connector to 22.1032.1.Q71 [follow ME connector list]	2010/7/5	P.14[PCH (3 of 9)-DMI/FDI]	Change D3 to schottky diode.
2010/6/10	P.36[AD / BATT CONN]	Change DCIN1 to 20.F0693.006 (follow connector list)		P.37[Thermal / Fan Controllor]	Delete Q29,Q30 main source 84.T3904.C11, follow CARAVEL-CP design
	P.41[FUNCTION BD & POWER BD]	Change PWCN1 to 20.F0693.006 (follow connector list)	2010/7/6	P.53[UL CIRCUIT]	Rename R642 Pin1 contact to RTC_BAT_1 (Old use RTC_BAT),follow CARAVEL-CP
2010/6/11	P.41[FUNCTION BD & POWER BD]	Del FUNCN2 connector by ME request			
	P.38[KBC_NPCE781L / KB]	Change R240 to 20K ohm SB version.			
	P.25[HDMI CONN_PS8101]	Change R614--R617 to 200R2J , Set mount. [for EMI request]			
	P.25[HDMI CONN_PS8101]	Change C283,C364 to 1uF [for EMI request]			
	P.25[HDMI CONN_PS8101]	Change C282,C285 to 1KpF [for EMI request]			
2010/6/21	P.16[PCH (5 of 9)-PCI/USB]	Add PCL_REQ2# Pull-High to 3D3V_S0 by hang-up issue			
	P.31[Audio Codec ALC269]	Change EC23,EC24 to mount [for EMI request]			
	P.55[EMI/Spring/Boss]	Change DCBATOUT capacity to mount (EC71--83,EC89,EC90,EC124,EC164--169) [for EMI request]			
		Change 5V_S0 capacity to mount (EC173--EC175) [for EMI request]			
		Change 3D3V_S0 capacity to mount (EC91--94,EC104) [for EMI request]			
		Change 3D3V_S3 capacity to mount (EC84--87) [for EMI request]			
		Change VCC_GFXCORE capacity to mount (EC142--146) [for EMI request]			
		Change VCC_CORE capacity to mount (EC136--139) [for EMI request]			
	P.36[AD / BATT CONN]	Change BT+ capacity to mount (EC32--35) [for EMI request]			
	P.23[LCD CONN]	Change C258 to 470pF (BRIGHTNESS_CN) [for EMI request]			
	P.34[CardReader RTS5186]	Add C272 between BLON_OUT_R and Gnd [for EMI request]			
		Change C576--580,C589 to 5pF [CardReader VEVs test]			
	P.24[CRT CONN]	Add 0.1uF between MS_INS# and GND [CardReader VEVs test]			
		Change R114,R115,R119,R120 to 2.7K ohm [CRT VEVs report]			
2010/6/22	P.53[UL CIRCUIT]	UL Circuit modify. [Prevent the RTC_BAT keep protecting.]			
2010/6/23	P.40[TouchPad]	Change THPAD1 to 20.K0487.006 [Follow ME connector list]			
	P.55[EMI/Spring/Boss]	Change SPR3 to DY [for EMI request]			
	P.53[UL CIRCUIT]	Add D42(83.00400.D1F), D41(83.00400.D1F) components. [Reduce the RTC_BAT discharge]			
		connect R467 pin1 to D41 and D42 pin k. [Reduce the RTC_BAT discharge]			
		connect D42 pin A to AD+_in. [Reduce the RTC_BAT discharge]			
	P.46[ADP3211_CPU CORE]	connect D41 pin A to ACP_UVP [Reduce the RTC_BAT discharge]			
		Change U45 to 84.08030.037 [Improve High side Vgs induce voltage]			
		Change U47 to 84.08028.037 [Improve High side Vgs induce voltage]			
		Change U48 to 84.08028.037 [Improve High side Vgs induce voltage]			
		add these statements. [follow Power Team design]			
	P.47[RT8223_5V/3D3V]	Change R316 to 7.87K ohm (old use 7.32K ohm) [Tune CPU Imon value]			
		Change C465 to 680pF (old use 560pF) [Tune CPU load line value]			
		Change R353 to 84.5K ohm (old use 97.6K ohm) [Adjust OCP value]			
		Change L13 to 2.2uH (old use 3.3uH) [IC needs higher sensing voltage to detect it.]			
	P.48[RT8209_1D5V]	Change R377 to 7.5K ohm (old use 11.5K ohm) [Adjust OCP value]			
	P.49[RT8209_1D05V]	Change R389 to 14.3K ohm (old use 10.2K ohm) [Adjust OCP value]			
		Change L15 to 0.56uH (old use 0.45uH) [Reduce the output ripple voltage]			
	P.50[ADP3211_GFX_CORE]	Change R419 to 56.2K ohm (old use 53.6K ohm) [Tune GFX load line value]			
		Change TC26 to mount.(old Dummy) [Improve under-shoot voltage phenomenon]			
2010/6/25	P.13[PCH (2 of 9)-PCIE/CLK/SMB]	Change C156,C157 to 12pF [for Crystal vendor Test]			
	P.29[LAN AR8131M]	Change C346 to 18pF [for Crystal vendor Test]			
	P.34[CardReader RTS5186]	Change C384,C388 to 15pF [for Crystal vendor Test]			
2010/6/29	P.17[PCH (6 of 9)-GPIO/RSVD]	Change RN31 to R648,R649 (56 ohm) for pull-high 1.05V_S0			
		Del R295 , because double pull-high			
2010/6/30	P.41[FUNCTION BD & POWER BD]	Change pin define of the FUNCN1 connector [follow the way of FFC folder for ME]			
	P.19[PCH (8 of 9)-PWR\SATA\USB]	Del R101 , only use 3D3V_S5			
	P.12[PCH (1 of 9)-SATA/RTC/HDA]	Change D1 to 83.R2003.I81 (SCHOTTKY DIODE)			
	P.25[HDMI CONN_PS8101]	Change Q12 to 84.2N702.D31 (ESD Protected 1.0KV)			
	P.44[RUN POWER]	Change D27 to 83.R2004.B8F (schottky diode)			
2010/7/1	P.46[ADP3211_CPU CORE]	Change OPEN-GAP to CLOSE-GAP (G9--14)			
	P.47[RT8223_5V/3D3V]	Change OPEN-GAP to CLOSE-GAP (G18,G22,G26,G30,G20,G24,G28,G32)			
		Change OPEN-GAP to CLOSE-GAP (G19,G23,G27,G31,G34,G36)			
		Change OPEN-GAP to CLOSE-GAP (G21,G25,G29,G33,G35,G37,G38)			
	P.48[RT8209_1D5V]	Change OPEN-GAP to CLOSE-GAP (G47,G49,G51,G53)			
		Change OPEN-GAP to CLOSE-GAP (G43--46,G48,G50,G52,G54--56)			
	P.49[RT8209_1D05V]	Change OPEN-GAP to CLOSE-GAP (G57,G58,G60,G62)			
		Change OPEN-GAP to CLOSE-GAP (G59,G61,G63--80)			
	P.50[ADP3211_GFX_CORE]	Change OPEN-GAP to CLOSE-GAP (G81--86)			
	P.51[RT8015_1D8V/ RT9026_0D75]	Change OPEN-GAP to CLOSE-GAP (G90--95)			
	P.41[FUNCTION BD & POWER BD]	Add F7 POLYSW for POWER BD 5V_S5 protect.			
	P.54[UVP Protect]	Delete R483 and add RN66. (RN66 part number is 66.10436.04L)			
		Connect AD+_IN to RN66 pin 1.			
		Connect RN66 pin2 to GND.			
		Connect RN66 pin3 and pin4 to AD+_SW_OFF_G_1			
	P.53[UL CIRCUIT]	Change R468 part number to the 64.36025.6DL			
		Change R469 to the part number 64.30025.6DL			
		Cummy R471 and mount D39.			
		Delete D40 and RN58.			
		Add R642. (Part number is 64.10045.6DL)			
		Connect R642 pin 1 to RTC_BAT.			
		Connect R642 pin2 to Q52 pin 2 and pin3.			
		Connect ACP to R435 pin 1.			
	P.52[BQ24751_Charger]	UPDATE BTCN1 PCB LAYOUT (REMOVE THE NPTH)			
	P.27[Bluetooth]				

<Core Design>

緯創資通		Wistron Corporation	
21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsueh,		Taipei Hsien 221, Taiwan, R.O.C.	
Title			
HISTORY EVT			
Size	Document Number		Rev
A2	TUCANA		SB
Date: Wednesday, July 07, 2010			
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